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A 1.8 μW Area-efficient Bio-potential Amplifier with 90 dB DC Offset Suppression

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Abstract—An area-efficient and low-power low-noise amplifier with adjustable parameters for bio-potential recording applications is presented. This amplifier replaces traditional analog filters using large AC coupling capacitor with the proposed DC offset suppression block based on Differential Difference Amplifier (DDA) structure, which allows the system to obtain good high pass characterization without using any area-consuming capacitors or resistors. It features configurable gain and bandwidth, which is suitable for various bio-potential applications and massive integration in biomedical devices. More than 90 dB DC offset suppression ratio is achieved in rejecting large DC offset and baseline drift that exist at the skin-electrode interface. The proposed bio-amplifier, designed in a 0.18 μm CMOS process and occupies only 0.027 mm² silicon area on chip, provides adjustable mid-band gain of 35.5/41.5/47.6/53.6 dB, tunable bandwidth from 0.01 Hz to 10 kHz. The back-annotated simulation results demonstrated the input-referred noise of 5.4 μVrms over 0.01 Hz-10 kHz and the total power dissipation consumed as low as 1.8 μW at 1.2 V power supply.

Keywords—bio-amplifier; bio-potential recording; DC offset; DDA; biosensor.

I. INTRODUCTION

Bio-amplifiers which are used to detect and amplify bio-potential signals are crucial and important Front-End blocks of portable biomedical systems. Biomedical signals are usually characterized by their low amplitude and low frequency behavior. To cater the acquisitions of different types of bio-potential signals, it is desirable have amplifiers to possess configurable gain as well as bandwidth. Moreover, to record neural signal from multiple sites simultaneously, one Front-End chip may have hundreds of arrayed data acquisition channels, which dominate the chip area and power budget in current implementations [1], [2]. Future devices should target the integration of much more on-chip processing circuits than just single amplifier per channel [3]. Furthermore, another critical problem facing integrated bio-amplifier is that of the large DC offset caused by the electrode interface, which may reach hundreds of millivolts. In some cases, large area-consuming capacitors and resistors were employed to remove the DC offset, thus restricting integration of the amplifier in large quantity (e.g. implantable multichannel neural recording systems). Therefore, the power, noise, size, DC offset as well as configurable structure are the major problems faced by high performance bio-amplifier design.

Although a significant amount of research has been devoted to address the above challenges, only a few reported designs meet the DC cancellation, power and size requirements for integration in a single front-end chip. Among the DC suppression schemes, capacitor feedback network with AC coupling of input devices to block the DC offset is popular in previous designs [4], [5], [10-12]. The main drawbacks of this capacitors AC coupling approach are degraded input-referred noise, lowered the input impedance of the amplifier, and caused possible mismatch in passive input devices. More significantly, this configuration requires very large capacitors which occupy considerable chip area to achieve satisfactory gains. Chopper stabilization scheme is also a creditable technique to obtain high noise performance and DC offset rejection [6], but it consumes more power as the circuit is working in the chopping frequency and additional circuitries like modulator and clock generator are needed. Another important technique is to employ MOS-bipolar pseudo-resistor element in parallel with a capacitive feedback to provide a low frequency. However, the MOS-bipolar resistance between input and output is highly dependent on the large output signal level, which results in distortion [2]. The forward DC cancellation scheme based on MOS pseudo-resistor can be utilized to create an RC high pass filter [7]. The amplifier can achieve DC offset rejection as well as small size without large passive devices. However, the amplifier works in the open-loop mode in the midband, and the gain suffered from the variation of the open-loop gain of low noise amplifier, which would be more severe in multichannel applications.

This paper try to design an amplifier that combines the new DC offset suppression scheme to the Differential Difference Amplifier (DDA) structure avoid using any input large AC coupling capacitors to achieve low cutoff frequency, good system linearity as well as compacted chip size. The amplifier is also optimized for low power, low noise, and with a tunable gain/bandwidth.

II. CIRCUIT IMPLEMENTATION

Fig. 1 shows the schematic of the proposed bio-amplifier which consists of a low-noise DDA, bandwidth (BW) and gain tuning blocks. The DC offset suppression is implemented in the BW block by adopting diode-connected MOS pseudo-resistors (M1 and M2) at the input of DDA along with the input PMOS gate capacitor (Cg) to create an RC high pass filter first introduced in [7]. Its time constant sets the low 3-dB cutoff
frequency of the bio-amplifier. The midband gain of the bio-amplifier equals the ratio of resistors in the feedback network. This negative feedback loop senses the reference voltage at node \(V_{\text{ref}}\) and provides a stable common mode voltage for output of the bio-amplifier, which makes this structure more robust.

![Fig. 1 Schematic of the proposed bio-amplifier.](image)

### A. DC Offset Suppression Scheme

The basic principle of this DC offset suppression scheme is mainly based on the two signal paths to the input terminal \(V_{pp}\) and \(V_{pn}\) of DDA in Fig. 1, where the amplitude and phase characteristics through each path are the same for DC but different for the AC signal. DC offset would be suppression by subtracting between the positive terminal \(V_{pp}\) and negative terminal \(V_{pn}\) while the signal would not (see Fig. 2). In this design, subthreshold biased MOS transistors M1 and M2 along with the parasitic capacitors of the negative terminal of the DDA provide a low frequency pole which result in a large time constant \(\tau\).

![Fig. 2 Subtracting the DC component from the amplifier input yields a DC offset suppression circuit.](image)

From Fig. 2, the transfer function of the bio-amplifier can be given by

\[
H(s) = \frac{A_0}{s + A_0 R(s)},
\]

where \(A_0\) is the open-loop gain of the DDA, \(R(s)\) is the gain function of resistors feedback network. The transfer function yields a lower cutoff frequency of

\[
f_{-3\text{dB low-cutoff}} = 1/2\pi \tau ,
\]

where \(\tau = R_f C_p\), \(R_f\) is the resistance of MOS-bipolar pseudo-resistor provided by transistors M1 and M2 and \(C_p\) is the parasitic capacitor of input transistor in DDA. Equation (2) denotes the associated low-frequency cutoff. It should be noted that the DC voltage across M1 and M2 is maintained at approximately the same value since there is no DC path between them and they are only connected with the gate capacitor of the input transistor in DDA input stage. Hence, the design can achieve good system linearity.

### B. Differential Difference Amplifier (DDA)

The DDA is a continue-time five-terminal operational amplifier structure with four multi-input terminals [8]. Fig. 3 shows the simplified schematic of proposed DDA, which consists of biasing stage, current-mirror OTA stage and gain operational amplifier stage. The open-loop relationship between input and output is expressed as

\[
V_{out} = A_0 \left[ (V_{pp} - V_{pn}) - (V_{np} - V_{nn}) \right],
\]

where \(A_0\) is the open-loop gain of the DDA. Suppose the DDA has infinite open-loop gain, and then the differential voltage of the two input ports become equal, i.e.

\[
V_{pp} - V_{pn} = V_{np} - V_{nn}.
\]

In order to reduce noise and power consumption, PMOS transistors with larger sizes and working in the subthreshold region of the input stage are used in this amplifier design. It obtains larger \(g_m\) value and achieves low frequency flicker noise.

![Fig. 3 Schematic of the proposed DDA.](image)

### C. Gain and Bandwidth Tuning

The midband closed loop gain of the bio-amplifier \(A_v\) is determined by the resistors feedback configuration as shown in Fig.1 and according to equations (3) and (4), the closed-loop gain expression is given by,

\[
A_v = 1 + \frac{A_0}{R_f}.
\]

Therefore, the midband gain of the bio-amplifier can be adjusted by the external control bits S1 and S0 which select different values of the feedback resistor \(R_f\) array.

For tunable low cutoff frequency, voltage-controlled MOS transistors (M1 and M2) working in subthreshold region are adopted, which can permit low-frequency cutoff tuning by external voltage \(V_b\) in Fig.1. The drain current of M1 and M2 can be found from [9]:

\[
I_{\text{sub}} = \frac{W}{L} I_0 e^{\frac{V_{gs} - V_{th}}{m V_T}} \left( 1 - e^{-\frac{V_{ds}}{V_T}} \right),
\]

where \(I_0 = qX D_n n_{p0} e^{kT/V_T}, V_T = kT/q, \) and \(V_{th}\) is the threshold voltage of MOS transistor, and index \(n\) is the subthreshold swing factor. The drain current passes through the diode-connected M1 and M2 with large \(L\) is relatively
small, which yields a relatively large resistor \((10^{14} - 10^{16} \Omega)\) since the current is pretty weak. By varying external control voltage \(V_b, I_{sub}\) and hence the equivalent resistance, a tunable low-cutoff frequency can be achieved.

D. Noise Analysis

Flicker noise and thermal noise in the circuit will degrade significantly the signal to noise ratio (SNR) in the bio-potential recording. The equivalent input-referred noise model of the proposed bio-amplifier is given by

\[
\frac{V_{n,\text{total}}^2}{V_{n,\text{DDA}}^2} = \frac{V_{n,\text{DDA}}^2}{A_v^2} + 4kT R_{eqm} \cdot \Delta f,
\]

where \(V_{n,\text{DDA}}^2\) is the output noise power of DDA, \(R_{eqm}\) is the equivalent resistor of MOS-bipolar transistors M1 and M2 and \(\Delta f\) is the recording bandwidth. The total system noise is also related to the recording bandwidth. 1/f noise is dominant for low bandwidth, while the thermal noise becomes dominant as the bandwidth increases. Therefore, the bio-amplifier is designed such that its high pass performance could generate a low 1/f noise. In this design, large area of the PMOS transistors are used in the differential input stage of the DDA which can decrease flicker noise effects as well as increasing the parasitic capacitor for the low cutoff frequency pole.

III. Simulation Results

The compacted low-power bio-amplifier is designed in 0.18 \(\mu\)m standard CMOS process. It occupies only 0.027 mm\(^2\) \((200 \mu\text{m by } 135 \mu\text{m})\) of the chip area and dissipates around 1.5 \(\mu\)A from 1.2 V power supply with the largest bandwidth settings. All the results presented below are based on the back-annotated simulation with HSPICE.

A. DC Offset Suppression

The AC response of this bio-amplifier is shown in Fig. 4. It exhibits passband from 0.01 Hz to 10 kHz with a gain of 35.5 dB. The DC offset suppression ratio of the bio-amplifier is about 90.2 dB.

B. Close-Loop Gain

Fig. 5 shows the close-loop gains of the bio-amplifier selectable by the 2-bit digitally control signal. The figure shows the gain changed by varying the two bits-S1S0. The four combinations of S1S0 can set the midband gain to 35.5 dB, 41.5 dB, 47.6 dB and 53.6 dB.

C. Low-cutoff Frequency

The bio-amplifier frequency response with tunable low-cutoff frequency is shown in Fig. 6. The gain of the bio-amplifier is set to 35.5 dB and the results show that when control voltage \(V_b\) is changed from 0.6 V to 0.1 V, the low-cutoff frequency changes from 0.01 Hz to 250 Hz. Fine-tuning the low cutoff frequency is expected to obtain by external controlled voltage \(V_b\) if frequency drift is caused by process variation or mismatch among the different channels.

D. Noise Performance

The equivalent input-referred noise density in the frequency range of 0.01 Hz up to 10 kHz is shown in Fig. 7. Integration under this curve from 0.01 Hz to 10 kHz yields a total Root Mean Square (RMS) of input-referred noise voltage about 5.4 \(\mu\)VRms.

Noise Efficiency Factor (NEF) is used to compare different low noise bio-amplifier architectures. It is basically a figure of merit based on power-noise trade-off. NEF is defined as:

\[
NEF = \frac{V_{in,rms}}{\sqrt{\frac{2I_{total}}{8VT4kT\cdot BW}}}.
\]
previous designs. This addresses the typical restricted power which is competitive compared with other designs [4], [7], [10-12].

The robustness of the system architecture and employing new DC offset suppression schemes has been presented. The robustness of this design is determined to be 2.6, which is competitive compared with other designs [4], [7], [10-12].

Table I summarizes the performance of this work as compared to state-of-the-art designs. By carefully engineering the system architecture and employing new DC offset suppression techniques, the area of the bio-amplifier is 0.027 mm² and the power consumption is only 1.8 μW with good noise and DC offset suppression performance.

I. CONCLUSION

A low power fully integrated bio-potential amplifier with DC suppression scheme has been presented. The robust topology based on DDA structure and the use of pseudo-resistors provides stable close-loop gain as well as a low cutoff frequency of millihertz. The new DC cancellation scheme provides about 90 dB offset suppression which avoids employing area-consuming capacitors or resistors compared to previous designs. This addresses the typical restricted power and size budget in massive integration in medical devices and applications (e.g., multi-site neural signal acquisitions). Moreover, this design consumes a power of 1.8 μW and achieves the total integrated input-referred noise of 5.4 μVrms in the range of 0.01 Hz-10 kHz corresponding to 2.6 NEF, a tunable bandwidth from 0.01 Hz to 10 kHz and programmable gains 35.5/41.5/47.6/53.6 dB. The proposed bio-amplifier is expected to be applicable to the recording of various low frequency and low amplitude bio-potential signals.

REFERENCES

Table I Performance Summary and Comparison with Other Bio-Amplifier

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<td>0.5</td>
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<td>Cap. AC</td>
<td>Cap. AC</td>
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<td>Power (μW)</td>
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<td>(μV)</td>
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<td>NEF</td>
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*Calculated by author. Ref. [7] indicated that the current consumption is 22/1A with 1.5 μm CMOS process.

Back-annotated simulation results.

where $V_{in_{rms}}$ is the RMS of input-referred noise voltage, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $V_T$ is the thermal voltage (0.026 V@300 K), BW is the -3 dB bandwidth and $I_{total}$ is the total supply current of the bio-amplifier. The NEF of this design is determined to be 2.6, which is competitive compared with other designs [4], [7], [10-12].

Table I summarizes the performance of this work as compared to state-of-the-art designs. By carefully engineering the system architecture and employing new DC offset suppression techniques, the area of the bio-amplifier is 0.027 mm² and the power consumption is only 1.8 μW with good noise and DC offset suppression performance.

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