Improved Characteristics for MOHOS Memory with Oxygen-Rich GdO as Charge Storage Layer annealed by NH_3

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Abstract-Characteristics of metal-oxide-high-k-oxide-silicon (MOHOS) memories with oxygen-rich or -deficient GdO as charge storage layer annealed by NH_3 or N_2 are investigated. Transmission electron microscopy, X-ray photoelectron spectroscopy and X-ray diffraction are used to analyze the cross-section quality, composition and crystallinity respectively of the stack-gate dielectric with a structure of $Al/Al_2O_3/GdO/SiO_2/Si$. The MOHOS capacitor with oxygen-rich GdO annealed in NH_3 exhibits a good trade-off among its memory properties: large memory window (4.8 V at ±12 V, 1 s), high programming speed (2.6 V at ±12 V/100 μs), good endurance and retention properties (window degradation of 5% after 10^5 P/E cycles and charge loss of 18.6% at 85 ^{0}C after 10 year, respectively) due to passivation of oxygen vacancies, generation of deep-level traps in the grain boundaries of the GdO layer, and suppression of the interlayer between GdO and SiO_2 by the NH_3 annealing.

Keywords: MOHOS memory, charge storage layer, Oxygen-rich GdO, oxygen-deficient GdO, NH_3 annealing.

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1. Introduction

Charge-trapping flash memory device in a metal-oxide-high-k-oxide-silicon (MOHOS)-type structure with high-k dielectric as charge storage layer (CSL) has attracted much interest due to its advantages over the conventional floating-gate flash memory, e.g. easier scalability, lower operating voltage, and simpler fabrication process which is compatible with standard complementary metal-oxide-semiconductor technology [1]. Recently, rare-earth metal oxides have been extensively studied for flash memory applications because of their promising thermal, chemical, and electrical properties [2]. Gadolinium oxide (GdO) is an attractive candidate as CSL in the flash memory devices due to its thermodynamic stability, perfect lattice matching with Si [3], energy bandgap of > 5 eV, and dielectric constant of ~ 14 [4]. A wide energy bandgap is required to produce sufficiently high densities of trap states with deep energy levels for improving the charge-trapping efficiency [5]. Large dielectric constant can offer a larger voltage drop across the tunnel oxide. The good memory properties of GdO nano-crystals and Gd-incorporated HfO_2 dielectric as CSL have been reported [6, 7]. It is expected that good charge-trapping behaviors of the GdO itself as CSL could be obtained. On the other hand, nitridation during post-deposition annealing (PDA) in NH_3 can effectively suppress the formation of a low-k interlayer and obtain a smoother interface [8]. So, in this work, a capacitor memory with a structure of $Al/Al_2O_3/GdO/SiO_2/Si$ is proposed, and the effects of PDA in NH_3 on the structural and electrical characteristics of GdO as CSL are investigated.

2. Experiments

MOHOS and metal-high-k-oxide-silicon (MHOS) capacitors were fabricated on

(100)-oriented p-type Si wafers with a resistivity of 1-10 Ωcm. The wafers were cleaned with a standard Radio Corporation of America process, and then dipped in dilute 2% HF to remove the native oxide. A thin SiO_2 film as the tunneling layer was thermally grown in dry O_2 at 900 °C. Then, oxygen-deficient GdO and oxygen-rich GdO were deposited as CSL by reactive sputtering of Gd_2O_3 target at an Ar/O_2 flow ratio of 4/0 and 4/1, respectively. The samples were annealed in NH_3 or N_2 ambient at 550 °C for 2 min and denoted as GDON and GDO for the oxygen-deficient GdO samples, and GDOON and GDOO for the oxygen-rich GdO samples, respectively. Next, Al_2O_3 was deposited as blocking layer (BL) by atomic layer deposition method by alternating deposition cycles of $Al(CH_3)_3$ and H_2O precursors at 300 °C for the MOHOS capacitors only. Finally, Al was evaporated and patterned as gate electrode and also as back electrode, followed by forming-gas annealing in H_2/N_2 (5% H_2) at 300 °C for 20 min.

The crystalline structure, cross-section quality and composition of the GdO films were examined by X-ray diffraction (XRD), transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS), respectively. The electrical characteristics of the capacitors were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer. All electrical measurements were carried out under a light-tight and electrically-shielded condition. The flat-band voltage (V_{FB}) of the samples was extracted by assuming $C_{FB}/C_{OX} = 0.5$ (C_{FB} and C_{OX} are the flat-band and oxide capacitances respectively, determined from 1-MHz high-frequency C-V curve).

3. Results and discussion

The thickness and cross-section quality of the GdO/SiO_2 stack were determined and

confirmed by the TEM images shown in Fig. 1. The GdO/SiO_2 stack thickness is 6.0 nm/3.0 nm, almost consistent for the GDON, GDO and GDOON samples. However, for the GDOO sample annealed in N_2, the thickness of the tunnel layer is larger (~ 3.40 nm) due to a Gd-silicate ($GdSiO_x$) interlayer (~ 0.55 nm) formed between GdO and SiO_2, as shown in Fig. 1. This indicates that the oxygen incorporated by the sputtering diffuses to the GdO/SiO_2 interface during the N_2 annealing, resulting in the growth of an interfacial $GdSiO_x$ layer. On the other hand, such interlayer is not observed in the GDOON sample due to the blocking role of nitrogen incorporated during the NH_3 annealing [9].

Fig. 2(a) shows the Gd 4*d* XPS spectra of the four GdO samples. The Gd 4*d* spectrum shows two strong peaks of 4*d*5/2 and 4*d*3/2 at 142.42 eV and 148.51 eV, 142.34 eV and 148.51 eV, 142.03 eV and 148.44 eV, 142.81 eV and 148.89 eV for the GDO, GDON, GDOO and GDOON samples, respectively. The GDOON sample displays a shift toward higher binding energy compared to those of the other samples, indicating that Gd becomes more ionic and loses more charge [10] due to the sputtering process with oxygen incorporation and the PDA in NH_3 atmosphere. However, the peaks of the GDOO sample shift to a lower binding energy, suggesting that some Gd reacts with Si, resulting in a thin Gd silicate interlayer, which is consistent with the TEM results in Fig.1. Consequently, the process of cation oxidation and oxygen vacancy passivation would be incomplete by incorporating oxygen during the sputtering only. Moreover, since the nitrogen molecules during the PDA in N_2 cannot bond to oxygen interstitials, the low-k silicide interlayer could form as a result of oxygen interstitials diffusing from the GdO film to the GdO/SiO_2 interface [11].

The XRD patterns of these CSL films after the PDA treatment are presented in Fig. 2(b).

Due to the weak diffractive peaks, amorphous structure is the dominant one for the GdO films, comprising few crystalline grains. The (611) peak of cubic Gd_2O_3 is observed in all the samples, implying that it is the dominant crystal orientation after annealing at 550 °C in both NH_3 and N_2 atmospheres. In addition, a small (211) peak of cubic Gd_2O_3 for the GDON and GDOON samples and a small (311) peak of cubic Gd_2O_3 for the GDO and GDOO samples occur in the XRD pattern due to different annealing ambients.

Fig. 3 depicts the 1-MHz counterclockwise C-V hysteresis loop of the MOHOS capacitors under ±6 V sweeping voltage for the oxygen-deficient and oxygen-rich GdO samples without annealing. The sweeping is performed first from inversion to accumulation and then back to inversion. The large positive V_{FB} shift (2.4 V) of the oxygen-deficient GdO sample indicates the presence of negative trapped charges in its CSL, and the main intrinsic defect in the dielectric is probably oxygen vacancies, which could trap one or two electrons to form negative charge centers, causing a positive V_{FB} shift [12]. On the other hand, the small V_{FB} shift (1.2 V) of the oxygen-rich GdO sample implies that the incorporation of oxygen during sputtering can reduce oxygen vacancies in the GdO dielectric to some extent. Fig. 4 gives the memory window of the four samples under different program/erase (P/E) voltages for 1 s. The initial condition for programming is set after injection of holes by applying a negative gate bias to drive the memory to erase state, while the initial condition for erasing is obtained after electron injection by applying a positive gate bias to drive the memory to program state. The V_{FB} shift under each program or erase voltage is extracted from the C-V curve of different capacitors respectively. Since the PDA treatment in N_2 or NH_3 is not effective for passivating the oxygen vacancies [13], larger memory window is still obtained

for the GDON and GDO samples than for the GDOON and GDOO samples, though the window difference between both is small (around 0.5 V at different P/E voltages). So, it could be believed that the traps in the CSL of the annealed samples should be mainly from the grain boundaries of the small crystal grains confirmed in Fig. 2(b), as well as from the residual negatively-charged oxygen vacancies. Moreover, the larger memory window of the samples annealed in NH_3 than that annealed in N_2 could be ascribed to creation of extra electron traps related to the hydrogen decomposed from the NH_3 gas [14].

The V_{FB} shift of the four samples as a function of programming/erasing time at P/E voltages of ±12 V is shown in Fig. 5. Minimum shift of V_{FB} is observed for the GDOO sample, indicating a limited amount of electron traps in its CSL. For the GDON and GDO samples, the V_{FB} shift gradually increases and is smaller than that of the GDOON sample until ~200 ms for the GDON sample and 1 s for the GDO sample, and beyond 500 ms, a quick increase of V_{FB} shift occurs, especially for the GDON sample. This change trend of V_{FB} implies a wide distribution of electron traps in the CSL of the two samples with more traps located near the CSL/SiO_2 interface because filling of the traps happens first near the gate side and then towards the SiO_2 side [15], thus leading to a low programming speed. For the GDOON sample, a large V_{FB} shift occurs for the initial 100 μs (74% of the saturation value), indicating a high programming speed, which should be associated with the high electron-trap density in the bulk of its CSL. For erasing operation, the V_{FB} of the GDON, GDO and GDOO samples increases continuously without saturation as erasing time increases, and even exceeds the initial V_{FB} value (-1.5 V) after 1 s for the GDON and GDOO samples, giving rise to an over-erase phenomenon associated with a large amount of hole trapping, which is

originated from the defect states in the dielectrics and interlayer [16]. However, it is observed that the negative V_{FB} shift of the GDOON sample becomes saturated after 1-s erasing with no over-erase phenomenon, indicating suppressed generation of hole traps due to the hardened CSL/SiO_2 interface achieved by the NH_3 annealing.

Fig. 6 shows the retention properties of the P/E states measured at a high temperature of 85 °C with an initial ±12 V/1-s P/E operation, which gives an initial window of 5.3 V, 4.7 V, 4.8 V and 4.4 V for the GDON, GDO, GDOON and GDOO samples, respectively. The extrapolated 10-year memory window is 1.53 V, 1.28 V, 3.25 V and 1.79 V, where the retention rate of electron charge for the program state is evaluated to be 36.8%, 34.2%, 81.4% and 50.7%, for the GDON, GDO, GDOON and GDOO samples, respectively. Obviously, the GDOON sample exhibits the best retention properties among the four samples, with the largest post-10-year memory window and the lowest charge loss rate. It is well known that thermal emission of electrons from traps is enhanced at a high temperature of 85 °C and the loss rate of electron charges from shallow traps is higher than that from deep traps [17, 18]. For the GDON and GDO samples, the high loss rate of trapped electrons for the program state could be attributed to the fact that the oxygen vacancies in the CSL act as shallow electron traps [19]. Moreover, the tendency of oxygen vacancies diffusing to and segregating at the CSL/SiO_2 interface provides a mechanism for subsequent formation of interfacial defect states [20]. This is an important leakage current source for the trap-assisted tunneling of trapped electrons, leading to poor charge retention. As compared to the GDOO sample, the better charge retention of the GDOON sample should be attributed to not only the reduced shallow-level traps resulting from nitridation-induced passivation of oxygen vacancies, but

also the suppressed formation of the interlayer between the CSL and SiO_2 by the NH_3 annealing. Since the interlayer formation consumes a little of SiO_2 and the $GdSiO_x$ interlayer has smaller barrier height than SiO_2, charge loss under the retention state would be increased [21].

Fig. 7 is the endurance characteristics of the MOHOS capacitors with ±12 V/100 ms pulse stress. The memory window after 10^5 cycles is 3.8 V, 3.1 V, 3.9 V and 4.0 V (the initial window is 4.0 V, 3.6 V 4.1 V and 3.9 V) for the GDON, GDO, GDOON and GDOO samples respectively. It can be seen that only a slight reduction or even an increase of memory window happens for these samples after stressing. Except for the GDOON sample, both program and erase V_{FB}'s of the other three samples obviously decrease as the cycle increases, suggesting enhanced electron detrapping and hole trapping by repetitive P/E stress. On the other hand, the I-V characteristics of the samples before and after a 10^5-cycle P/E stress are measured by using the MHOS capacitors, and the leakage current density of the GDON, GDO, GDOON and GDOO samples at a gate voltage of 1.5 V is 2.6 nA/cm^2, 3.1 nA/cm^2, 1.5 nA/cm^2 and 2.4 nA/cm^2 before stressing, and 3.1 nA/cm^2, 3.7 nA/cm^2, 1.7 nA/cm^2 and 3.3 nA/cm^2 after the P/E stressing, respectively. Smallest increase in leakage current after stressing for the GDOON sample indicates least de-trapping of electrons due to suppressed stress-induced defects (associated with nitrogen-related strong bonds created during the NH_3 annealing), resulting in best endurance properties.

4. Conclusion

In summary, MOHOS-type capacitor memories with a high-k GdO as charge storage layer are fabricated by sputtering in the presence or absence of oxygen, and the effects of PDA in

NH3 on their memory characteristics have been investigated. The stacked gate structure, cross-section quality and composition of the GdO films in the MOHOS capacitors are analyzed by means of TEM, XPS and XRD methods. It was found that the oxygen-rich GdO annealed in NH_3 ambient can achieve a good trade-off among the memory characteristics, showing large memory window (4.1 V at P/E voltage of ± 12 V for 100 ms), high programming speed, reasonable retention properties with an extrapolated 10-year electron charge loss of 18.6% at 85 ^{0}C and good endurance properties with 5% degradation after 10^5 P/E cycles. These improvements are attributed to crystallization-induced deep-level electron traps in the bulk of the CSL, reduction of shallow traps near the CSL/SiO_2 interface due to passivation of oxygen vacancies and suppressed formation of GdSiO interlayer by NH_3 annealing. Therefore, the oxygen-rich GdO dielectric with post-deposition annealing in NH_3 is a promising candidate as the charge storage layer for advanced MOHOS nonvolatile memory applications.

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Captions:

Fig. 1 TEM images of the stacked gate dielectric for the four annealed samples.

Fig. 2 Gd 4*d* XPS spectra (a) and XRD spectra (b) for the CSL films of the four annealed samples.

Fig. 3 C-V hysteresis measured at a sweep voltage range of ±4 V for non-annealed GdO samples.

Fig. 4 V_{FB} extracted from C-V curves under different P/E voltages for the four annealed samples.

Fig. 5 the change of V_{FB} as a function of P/E time for the four annealed samples.

Fig. 6 Retention characteristics of the four annealed samples measured at 85 °C.

Fig. 7 Endurance characteristics for the four annealed samples.

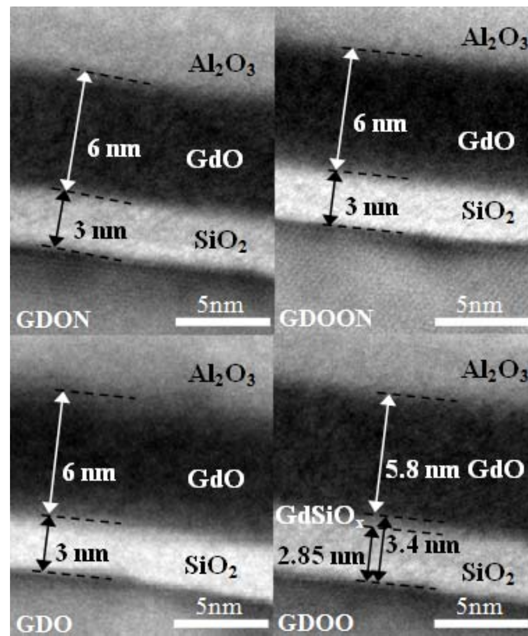

Fig. 1

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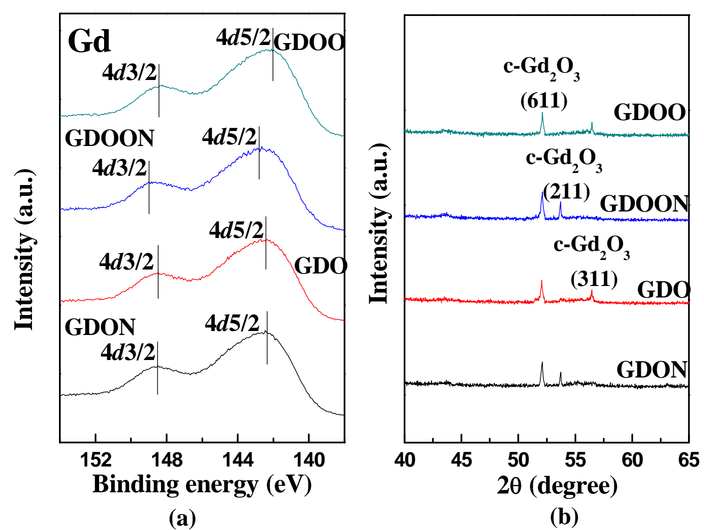

Fig. 2

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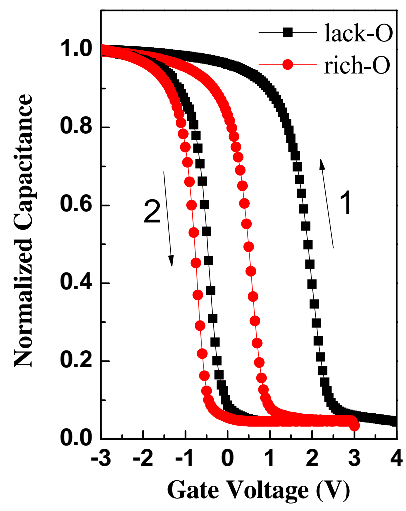

Fig. 3

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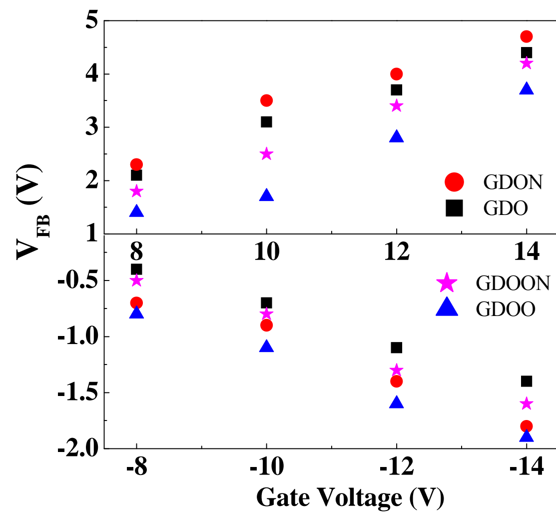

Fig. 4

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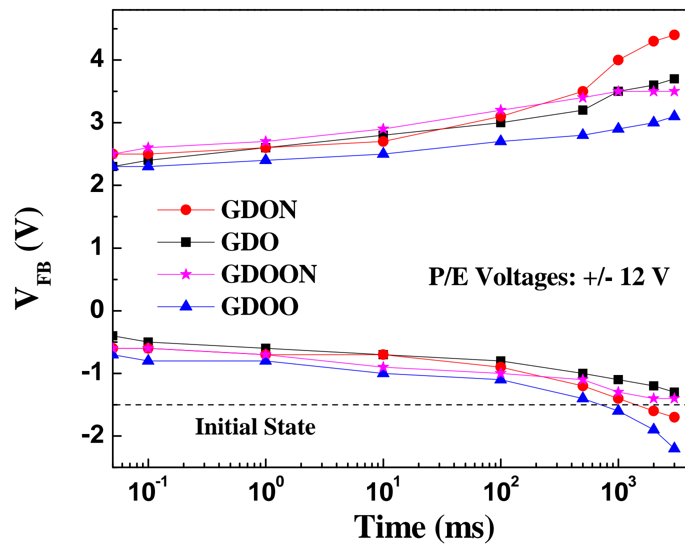

Fig. 5

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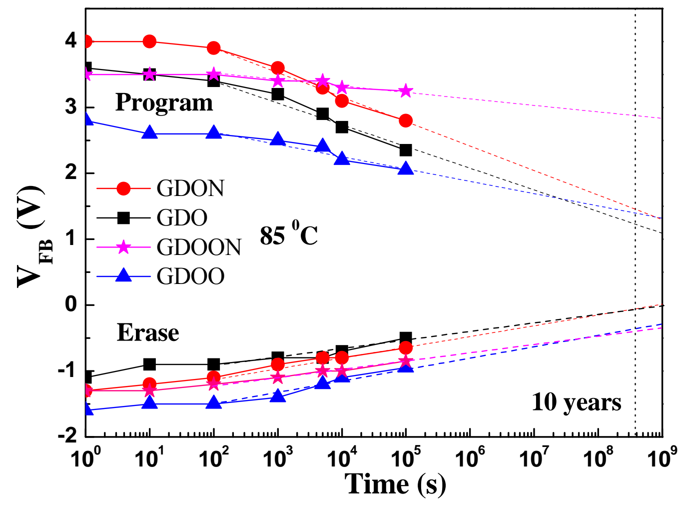

Fig. 6

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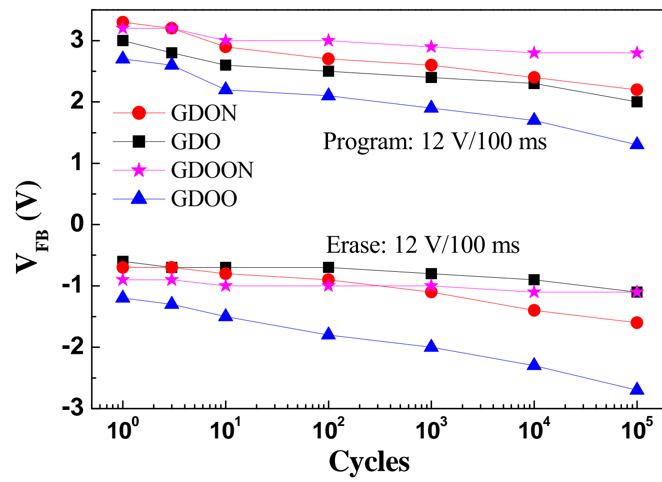

Fig. 7

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