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Improved charge-trapping properties of TiON/HfON dual charge storage layer by tapered band structure

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A TiON/HfON dual charge storage layer (CSL) with tapered bandgap structure is proposed for metal-oxide–nitride-oxide–silicon-type memory by using the inter-diffusion of Ti and Hf atoms near the TiON/HfON interface to form an intermixing layer of Hf_xTi_yON with varying Hf/Ti ratio in the dual CSL during post-deposition annealing, as confirmed by transmission electron microscopy. The memory capacitor with TiON/HfON as dual-CSL shows a large memory window of 5.0 V at ±12 V for 100 μs, improved cycling endurance with little degradation after 10^5 cycles and good data retention with an extrapolated 10-yr window of 4.6 V at room temperature. These are highly associated with the tapered bandgap structure and appropriate trap distribution in the dual CSL. Therefore, the TiON/HfON dual-CSL structure provides a very promising solution for future charge-trapping memory applications. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4754830]

Since conventional nonvolatile floating-gate memory device faces challenges and limits due to aggressive scaling trend beyond the 45 nm technology generation, metal-oxide–nitride-oxide–silicon (MONOS)-type memory has become an appealing alternative for next-generation flash memory applications due to its advantages such as film scalability, process simplicity, and power economy.[1,2] Nevertheless, some performance and reliability issues such as low charge-trapping efficiency, poor endurance, and short retention must be overcome before MONOS can be utilized in the semiconductor industry for future nano-scale flash memory device applications.[3] In order to further improve the scaling and relevant memory characteristics, extensive researches have been performed in recent years, involving the use of high-κ dielectrics as blocking layer (BL), charge storage layer (CSL) as well as tunneling layer (TL), and the barrier engineering of gate stacked structure due to different band offsets of dielectric materials.[4] In this work, a promising bandgap-engineering technique using high-k TiON/HfON as dual CSL in MONOS memory capacitor is proposed to improve the charge trapping properties. This involves the formation of a tapered bandgap due to the varying Hf/Ti ratio in the intermixing layer of the TiON/HfON stack causing different band offsets. It is demonstrated that good charge storage characteristics including high charge-trapping efficiency, improved program/erase performance and reliability can be achieved using the dual-CSL structure.

MONOS-type capacitors were fabricated on p-type (100) Si substrate with a resistivity of 5–10 Ω cm. After a standard Radio Corporation of America (RCA) clean, the wafers were dipped in diluted fluohydric acid (HF acid) for 1 min to remove the native oxide. A 3.5 nm thermal SiO_2 as TL was grown in dry O_2 at 900 °C on the surface of the wafers. Subsequently, a 5 nm TiON was deposited by reactive sputtering of Ti target in a mixed ambient of $Ar/N_2/O_2 = 12/15/3$. Following that, a 5 nm HfON was *in situ* deposited by reactive sputtering of Hf target in the same ambient. To form the Hf-Ti-O-N interlayer and improve the charge storage characteristics, a post-deposition annealing (PDA) treatment was carried out at a temperature of 550 °C for 1 min in N_2 ambient. Then, 12 nm Al_2O_3 was deposited as blocking layer by using the atomic layer deposition method. Al was evaporated and patterned as gate electrodes and also as back electrode. Finally, a forming-gas annealing was performed at 300 °C for 20 min. For comparison, MONOS capacitors with 10 nm HfON or TiON only as CSL was also fabricated using the same processing, and another sample with 10 nm-HfTiON as CSL was made by reactive co-sputtering of Hf and Ti targets in a mixed ambient of $Ar/N_2/O_2 = 12/15/3$. Accordingly, these samples are denoted as Ti/Hf (dual-CSL), Hf (single HfON as CSL), Ti (single TiON as CSL), and HfTi (HfTiON as CSL) samples, respectively.

The electrical characteristics of the four samples were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer. All electrical measurements were carried out under a light-tight and electrically shielded condition at room temperature. The flat-band voltage (V_{FB}) of the samples was extracted by assuming $C_{FB}/C_{OX} = 0.5$ (C_{FB} and C_{OX} are the flat-band and oxide capacitances, respectively, determined from 1 MHz high-frequency C-V curve).

The physical thickness of each dielectric layer was measured and confirmed by multi-wavelength ellipsometry and transmission electron microscopy (TEM). Fig. 1(a) is the cross-sectional TEM image for the dual-layer CSL with a high-κ TiON/HfON structure. It can be seen that an intermixing layer of Hf_xTi_yON with a varying Hf/Ti ratio is

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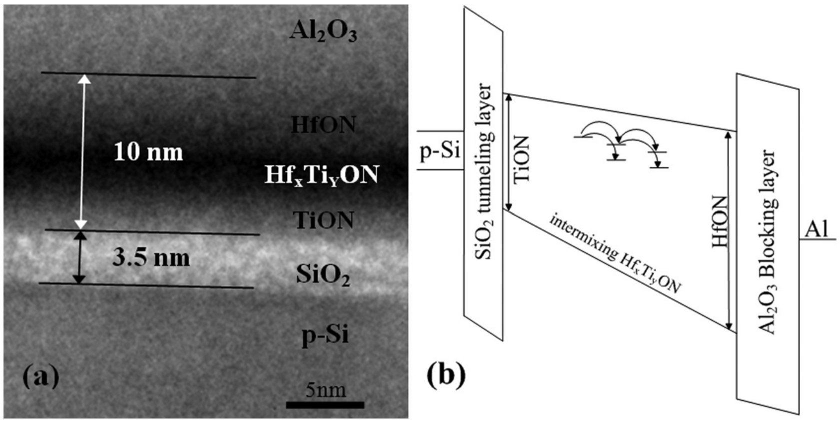

FIG. 1. TEM image of the stacked gate dielectric structure (a) and schematic diagram of energy band of the dual-CSL, where charge trapping mechanism during program operation is illustrated (b) for the Ti/Hf sample.

formed near the TiON/HfON interface due to inter-diffusion of the Ti and Hf atoms during the PDA. As reported in some recent articles,[5–7] the bandgap of Hf_xTi_yON is determined by the Hf/Ti ratio in the film, which should be larger than that of TiO_2 and smaller than that of HfO_2, and monotonously decreases with increasing Ti content.[6] So, a tapered bandgap should be formed due to Ti-rich Hf_xTi_yON in the TiON side and Hf-rich Hf_xTi_yON in the HfON side, as shown in Fig. 1(b). However, the non-uniform intermixing makes direct measurements of elemental composition and bandgap very difficult. As an alternative, the inter-diffusions of Hf and Ti in the mixed layer are analyzed by fabricating two dual-layer structures of TiON/HfON (5 nm/5 nm) and HfON/TiON (5 nm/5 nm) on Si substrate by annealing under the same conditions as above. As shown by the spectral peaks of Hf (4*f*) and Ti (2*p*) from x-ray photoelectron spectroscopy (XPS) in Fig. 2(a), the atomic ratio of Hf:Ti is estimated to be 6.8:1 for the HfON/TiON/Si structure and 1:7.8 for the TiON/HfON/Si structure, at a location of 2–4 nm below the surface (based on the x-ray penetration depth), i.e., inside the HfON layer of the former and inside the TiON layer of the latter. These results indicate that inter-diffusions of Hf and Ti occur during the PDA even at 550 °C for 1 min, thus confirming the formation of an intermixing layer of Hf_xTi_yON near the TiON/HfON interface, as shown in Fig. 1(a). Furthermore, three co-sputtered Hf_xTi_yON films for the Hf-rich (Hf:Ti = 5:1), Ti-rich (Hf:Ti = 1:6), and HfTi (Hf:Ti = 1:3) samples were deposited separately. The peaks associated with Hf (4*f*) and Ti (2*p*) are detected from the XPS spectra of the three Hf_xTi_yON films after the PDA treatment, as shown in Fig. 2(b). Compared with the values of 16.6 eV/18.2 eV for the Hf $4f_{7/2}$/Hf $4f_{5/2}$ peaks, as well as 458.3 eV/463.9 eV for the Ti $2p_{3/2}$/Ti $2p_{1/2}$ peaks, the Hf and Ti spectra show no significant changes for the different samples, implying that there is essentially no difference in chemical bonding for the Hf_xTi_yON films with different Hf/Ti ratios. So, HfON and TiON clusters in the Hf_xTi_yON composite films mix together with only structural changes but without new chemical bonds appearing,[6,8] basically independent of the co-sputtering method or PDA treatment. However, the bandgap and band offsets of Hf_xTi_yON change with the Hf/Ti ratio, resulting in different memory properties of TiON/HfON as dual CSL.

Fig. 3(a) depicts the 1 MHz counter-clockwise C-V hysteresis loop of the memory capacitors under ±4 V sweeping voltage. The Ti/Hf and HfTi samples exhibit significant V_{FB} shift (1.60 and 1.10 V, respectively), which is typical behavior for memory devices. On the other hand, the Hf and Ti samples show rather small V_{FB} shift (0.30 and 0.15 V, respectively), indicating low charge-trap density. The V_{FB} extracted from the C-V curve at different P/E voltages from ±8 to ±15 V is shown in Fig. 3(b). Much larger memory windows of the Ti/Hf and HfTi samples than those of the Hf and Ti samples are observed, indicating that a large quantity

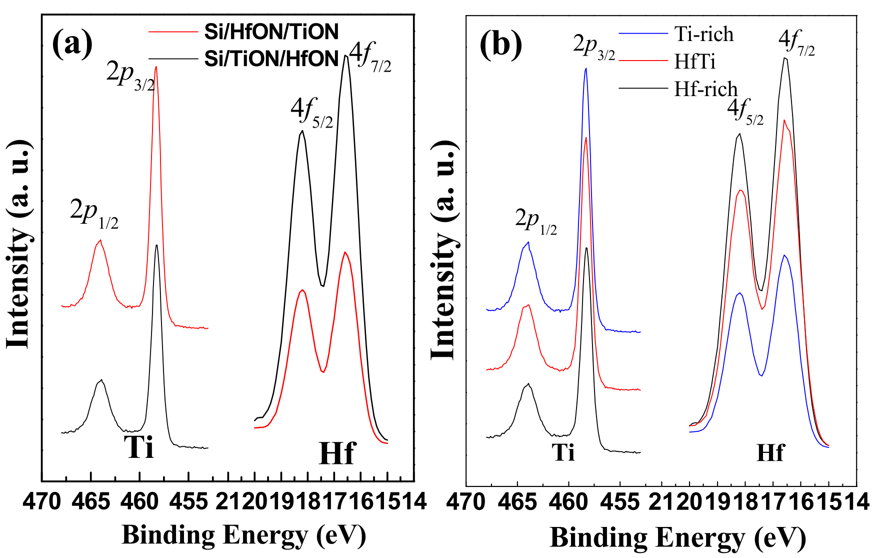

FIG. 2. XPS spectrum for the dual-layer structures of HfON/TiON/Si and TiON/HfON/Si (a) and three Hf_xTi_yON films with different Hf/Ti ratios (b).

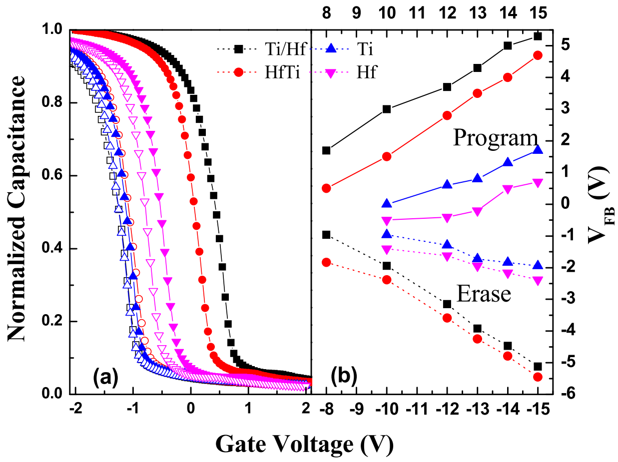

FIG. 3. C-V hysteresis curves of the four samples (a) and V_{FB} extracted from the C-V curves under different P/E voltages (b).

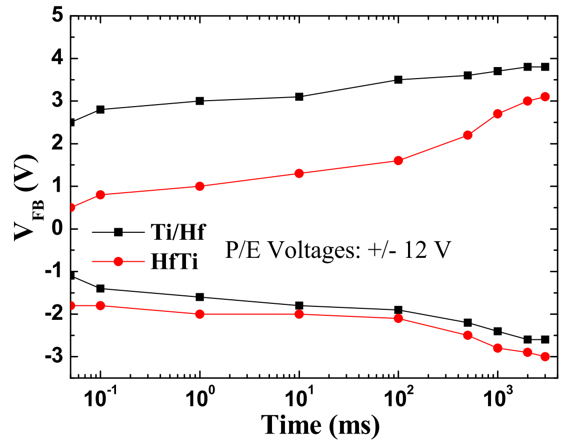

FIG. 4. Change of flat-band voltage of the Ti/Hf and HfTi samples as a function of P/E time.

of electron traps exists in the CSL of the Ti/Hf and HfTi samples due to the mixing of HfON and TiON, where strong electron trapping occurs in the samples containing significant amounts of both Hf and Ti.[8] Moreover, a gradually increasing bandgap from the TiON side to the HfON side in the CSL of the Ti/Hf sample increases the accessibility of deep trap levels. It is well known that shallow trap levels catch incoming charges easily while deep trap levels are buried underneath and may not be able to capture electrons easily.[9] On the other hand, the shallow trap levels cannot trap electrons tightly, causing insufficient stored charge. However, for the Ti/Hf sample, as shown in Fig. 1(b), a multi-level trap distribution probably exists in the tapered bandgap, and the substrate-injected charges are first caught by shallow trap levels and then migrating to deeper trap levels through lateral hopping. Thus, more trap levels are available for charge storage. In addition, the probability of the injected charges tunneling back to the substrate is reduced due to the increased barrier height between the CSL and the tunnel oxide (large conduction-band offset of TiON with SiO_2[10]), and the higher Ti content in the Hf_xTi_yON layer closer to the TL making the centroid of trapped electrons farther away from the dielectric/SiO_2 interface.[8] Overall, the charge-trapping efficiency of the Ti/Hf sample is greatly improved by its tapered bandgap, which can provide more and accessible charge-trapping levels for efficient charge storage.

The comparison of P/E transient characteristics between the Ti/Hf and HfTi samples is shown in Fig. 4 to investigate the effects of the tapered bandgap on operating speed. It can be seen that the V_{FB} shift of the Ti/Hf sample quickly reaches 3.0 V during the initial 100 μs programming time, indicating high programming speed and high trapping efficiency as compared to the HfTi sample with a distinct shift of V_{FB} only after 500 ms programming time. This is attributed to the large number of accessible trap levels, lower back-tunneling probability associated with the tapered bandgap structure, and the distribution of electron-trap energy levels in the TiON/HfON dual CSL, as mentioned above.

In order to evaluate device reliability, endurance characteristics are compared in Fig. 5(a). For the Ti/Hf sample, no observable endurance degradation occurs even after 10^5 cycles. For the HfTi sample, gradual decrease of the programming window and gradual increase of the erasing window with operating cycle should be due to deep-level hole traps near the CSL/SiO_2 interface generated by the P/E

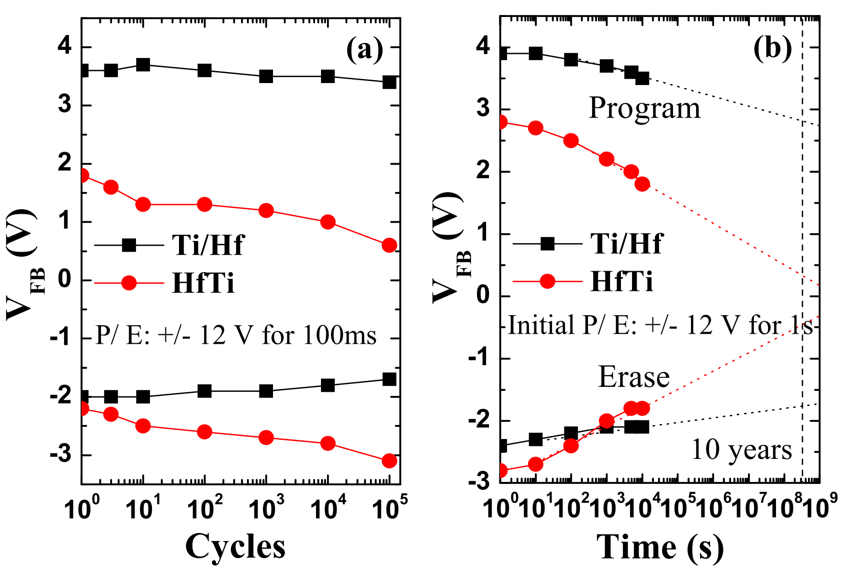

FIG. 5. Endurance with the P/E cycles (a) and retention characteristics at room temperature (b) for the Ti/Hf and HfTi samples.

stress, thus giving rise to accumulation of holes and blocking the injection of electrons. The good endurance of the Ti/Hf sample could be attributed to the highly accessible trapping levels and suitable energy-level distribution that allow charges to be trapped and de-trapped easily during the P/E operation. For the HfTi sample, an interfacial layer between HfTiON and SiO_2 probably exists because fast diffusion of oxygen vacancies in the hafnium oxide film would lead to an uncontrollable interfacial layer formed between the hafnium oxide film and substrate,[11] which is partly responsible for its poor electrical properties.[12] However, the Ti-rich oxynitride film can limit the release and diffusion of excess oxygen to the interface, thus suppressing the growth of the undesirable interfacial layer.[13] So, the Ti/Hf sample has an enhanced quality of the TiON/SiO_2 interface, which reduces the defects and undesired states generated near/at the interface during operation stress, thus resulting in excellent endurance characteristics.

The retention characteristics at room temperature are shown in Fig. 5(b). Keeping data for longer than 10 yr is another important reliability requirement of MONOS memory devices. The Ti/Hf sample exhibits a memory window of 4.6 V after 10 yr (27% loss of memory window), while that of the HfTi sample is only 0.8 V after 10 yr (85% loss of memory window). It is believed that the large 10-yr operating window of the Ti/Hf sample is associated with not only its superior performance at the beginning but also its very low loss rate of data due to its special band structure and trap distribution, large barrier height, and good quality of the CSL/tunnel oxide interface, thus resulting in excellent retention characteristics.

A highly efficient and reliable MONOS memory device has been developed by optimization of the CSL. Based on bandgap engineering, a MONOS capacitor memory with high-κ TiON/HfON as dual CSL has been proposed and fabricated. It is found that inter-diffusions of the Ti and Hf atoms near the TiON/HfON interface (forming a Hf_xTi_yON mixed layer with varying Hf/Ti ratio in the dual CSL) result in a tapered bandgap, and thus significant improvements of device performance and reliability have been achieved, e.g., high charge-trapping efficiency with a large memory window of 5.0 V at $\pm$ 12 V for 100 μs, improved cycling endurance with little degradation after 10^5 cycles, and good data retention with an extrapolated 10-yr window of 4.6 V at room temperature. Therefore, the TiON/HfON dual-CSL structure provides a very promising solution for future charge-trapping memory applications.

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