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(54) Title: RECTANGULAR CONTACT LITHOGRAPHY FOR CIRCUIT PERFORMANCE IMPROVEMENT

(57) Abstract: An optical lithography method is disclosed that uses double exposure of a reusable a chromeless alternating phase-shifting template mask and a binary trim mask to fabricate regularly-placed rectangular contacts in standard cells of application-specific integrated circuits (ASICs). A first exposure of the reusable chromeless alternating phase-shifting template ask forms periodic dark lines on a wafer and a second exposure of binary tri mask remove the unwanted part of the dark lines and the small cuts of the dark lines left form the rectangular-placed contacts. All contacts are placed regularly in one direction while randomly in the perpendicular direction. The method of the invention can be used in the fabrication of standard cells in application-specific integrated circuits (ASICs) to decrease circuit area an improve circuit performance.

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RECTANGULAR CONTACT LITHOGRAPHY FOR CIRCUIT PERFORMANCE IMPROVEMENT

FIELD OF THE INVENTION

The present invention relates to optical lithography. More specifically, the invention relates to a double-exposure photolithography method using a reusable alternating phase-shifting template mask and a trim mask to image regularly-placed rectangular contacts. The method of the invention can be used in the fabrication contact layer of standard cells in application-specific integrated circuits (ASICs) to decrease circuit area and improve circuit performance.

BACKGROUND OF THE INVENTION

The continuous demand for high speed integrated circuits (ICs) results in the continuous increase of transistor density and decrease of the feature size in the past two decades. The critical dimension (CD)---the minimum feature size that can be defined by optical lithography---has been reduced to 130\,nm at the end of the last century and is projected to reach the 65\,nm node in 2007. As a function of three parameters, the $CD(=k_1\frac{\lambda}{NA})$ is proportional to the wavelength of the exposure light λ and the process-related factor k_1, and decreases with increasing numerical aperture (NA) of the projection system. Over the past two decades, the development of optical lithography has been successful in reducing the λ from 436nm in the 1970s to 157nm in 2004 and increasing the NA to above 0.85. However, these improvements alone are

insufficient to reduce the feature size exponentially as projected by Moore's law.

As the third parameter and the best measure of lithography aggressiveness, the k_1 factor is the only parameter that can be controlled by lithographers for a given exposure system. The theoretical lower limit of the k_1 factor is 0.25. Over the past two decades, the k_1 factor has been reduced by over 0.1 every 5 years. Because image quality degrades noticeably when k_1 falls below 0.75, resolution enhancement techniques (RETs) such as modified illumination, optical proximity correction (OPC), and phase-shifting masks (PSMs) have been used to improve image quality for low- k_1 lithography. These RETs have been successful in reducing the k_1 factor to about 0.5. However, with k_1 approaching its limit, the additional improvement requires communications between the technology and the design communities. By considering circuit manufacturability in the layout design, it is expected that the k_1 factor can be further reduced by regularly-placed layout in which the circuit pattern configurations are limited to facilitate lithography optimization.

Contact and gate levels are the most difficult parts of a lithography process and have the biggest cost weighting. Many advanced lithography approaches have been proposed in the last few years for the contact and the gate level [BT02], pushing the k_1 to about its minimum value. All of these approaches require a regular placed contacts or gates.

There is a trade-off between randomly-placed (traditional) and regularly-placed (regularly-placed) layout. Excessive lithography friendliness may be so restrictive on layout compaction that circuit area increases unacceptably. Although the features can be designed smaller and packed

closer in regularly-placed layout, the initial area increase should be small enough such that it can be offset by shrinkage of the feature size.

Whether a circuit area will be smaller or not after using a regularly-placed layout depends on the applications. The layout strategy of regularly-placed layout should be determined according to the application.

In the application of regularly-placed contacts in standard cells, one of the core blocks of cell-based application-specific integrated circuits (ASICs), the contact should the placed randomly in the height direction while regularly in the width direction with ½ transistor pitch as the grid pitch (A transistor pitch, also called a "contacted pitch", is the minimum pitch between two gates with a contact between them.). That is because MOSFETs in a standard cell are placed one by one in the width direction. The width of a cell is roughly determined by the product of the transistor pitch and the number of the transistors. Reduction of the contact size gets a reduced transistor pitch and leads to a decrease of the cell width. On the other hand, it is the metal-1 pitch instead of the contact pitch or size that determines the height of a standard cell. The minimum pitch and size of contacts in the height direction is not critical for the height of standard cells. Applying a regular placement on the contacts in the height direction cannot help to decrease the height of a standard cell except for an increased difficulty in the layout compaction.

However, there are several difficulties to apply such a regularly-placed layout on a standard cell. Firstly, all of the approaches in the literature placed contacts regularly in both directions at the same time [BT02, WJ03]. Secondly, although the width resolution (single-exposure) can be improved by a regularly-placed layout, the desired width grid pitch (½ transistor pitch) is

still smaller than the improved resolutions of contact layer. Multiple exposures are introduced to fabricate the new layout [WJ03]. This increases the cost and decreases the throughput. The lithographic approach should be selected carefully to decrease the number of extra masks and exposures.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a lithography method by which circuit area and performance of standard cells in application-specific integrated circuits (ASICs) is improved.

It is another object of the present invention to provide a lithography method using double-exposure of a reusable chromeless alternating phase-shifting template mask and a trim mask for contact fabrication.

It is yet another object of the present invention to provide a lithography method by introducing less extra restrictions in layout design when apply regularly-placed contacts on design of standard cells in application-specific integrated circuits (ASICs).

It is yet another object of the present invention to provide a lithography method for regularly-placed contact fabrication with no extra specific mask needed.

One embodiment of the present invention is directed to a method of optical lithography wherein rectangular contacts placed randomly in one direction while regularly in the perpendicular direction characterized by a grid pitch, the grid pitch being selected to minimize the circuit area increase caused by the use of the grid, are printed to the wafer by double exposures by a reusable chromeless alternating phase-shifting template mask and a binary

trim mask. The rectangular contacts have a smaller dimension in the direction in which contacts are placed regularly.

A reusable chromeless alternating phase-shifting template mask is exposed first. The opposite phase shift of patterns on the chromeless phase-shifting template mask creates periodic unexposed dark lines at the boundary of 0° and 180° regions. The period of the 0° and 180° regions on the chromeless alternating phase-shifting template mask is design to be one transistor pitch so that the period of the dark lines is half of that. The Exposure of a binary contact trim mask on these periodic dark lines remove the unwanted parts of the dark lines and the small cuts of the dark lines left form the regularly-placed contacts.

Contacts are placed regularly in the width direction and randomly in the height direction in this invention. The size and location of contacts in the width direction are determined by the exposure of the reusable chromeless alternating phase-shifting template mask, while the size and location of contacts in the height direction are determined by the trim mask. Because the features in the trim are placed randomly, the location of contacts in the height direction are also randomly. Determined by the exposures of the different masks, the size of contacts is different in different directions. Using of regular placement and chromeless phase-shifting mask in the width direction, the size of contacts in the width direction is much smaller than the size of contacts in the height direction which is determined by the resolution of the exposure of the binary mask.

There are 2 masks (1 reusable template mask and 1 specific trim mask) and 2 exposures are needed to fabricate the rectangular regularly-placed

contacts in standard cells. Since there is no extra specific mask needed comparing with the ordinary lithography method for randomly-placed contacts, the extra cost is kept to the lowest.

A regular placement of contacts enables more effective use of resolution enhancement technologies, which in turn allows a reduction of the minimum contact size and pitch. However, the extra restrictions in layout increase the complexity of a layout design and might offset the benefits from the reduced contact size and pitch. Whether a circuit area will be smaller or not after using a regular contact placement depends on applications.

In the application of regularly-placed contacts in standard cells, one of the core blocks of cell-based application-specific integrated circuits (ASICs), the contacts should the placed randomly in the height direction while regularly in the width direction with ½ transistor pitch as the grid pitch (A transistor pitch, also called a "contacted pitch", is the minimum pitch between two gates with a contact between them.). That is because MOSFETs in a standard cell are placed one by one in the width direction. The width of a cell is roughly determined by the product of the transistor pitch and the number of the transistors. Reduction of the contact size gets a reduced transistor pitch and leads to a decrease of the cell width. On the other hand, it is the metal-1 pitch instead of the contact pitch or size that determines the height of a standard cell. The minimum pitch and size of contacts in the height direction is not critical for the height of standard cells. Applying a regular placement on the contacts in the height direction cannot help to decrease the height of a standard cell except for an increased difficulty in the layout compaction.

In this invention, rectangular contacts placed randomly in the height direction while regularly in the width direction characterized by a grid pitch, the grid pitch being selected to minimize the circuit area increase caused by the use of the grid, are printed to the wafer by double exposures of a chromeless alternating phase-shifting template mask and a binary trim mask. The rectangular contacts have a smaller dimension in the width direction.

A reusable chromeless alternating phase-shifting template mask is exposed first. The opposite phase shift of patterns on the chromeless phase-shifting template mask creates periodic unexposed dark lines at the boundary of 0° and 180° regions. The period of the 0° and 180° regions on the chromeless alternating phase-shifting template mask is design to be one transistor pitch so that the period of the dark lines is half of that. The Exposure of a binary contact trim mask on these periodic dark lines remove the unwanted parts of the dark lines and the small cuts of the dark lines left form the rectangular-placed contacts.

With the present method, the size and location of contacts in the width direction are determined by the exposure of the chromeless alternating phase-shifting template mask, while the size and location of contacts in the height direction are determined by the trim mask. Because the features in the trim are placed randomly, the location of contacts in the height direction are also randomly. Determined by the exposures of the different masks, the size of contacts is different in different directions. Using of regular placement and chromeless phase-shifting in the width direction, the size of contacts in the width direction is much smaller than the size of contacts in the height

direction which is determined by the resolution of the exposure of the binary mask.

There are 2 masks (1 reusable template mask and 1 specific trim mask) and 2 exposures are needed to fabricate the rectangular regularly-placed contacts in standard cell. Since there is no extra specific mask needed comparing with the ordinary lithography method for randomly-placed contacts, the extra cost is kept to the lowest.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described by reference to the drawings in which:

Fig. 1 is a diagram illustrating the structure of a standard cell;

Fig. 2a is a diagram showing the contact pitch distribution in the width direction for standard cells.

Fig. 2b is a diagram showing the contact pitch distribution in the height direction for standard cells;

Fig. 3 is a demo layout of rectangular contacts for the illustration of the invention;

Fig.4a is the chromeless alternating phase-shifting template mask for the second exposure;

Fig.4d is the exposure image of the template mask;

Fig.5a is Binary trim mask of the demonstration contacts for the second exposure;

Fig.5b is exposure image of the binary trim mask for the demo contacts; and

Fig.6 is the final image of the demo contacts by the overlap of the Fig.4b and the Fig.5b.

DETAILED DESCRIPTION OF THE PREFERRED AND ALTERNATIVE EMBODIMENTS

Fig. 1 is a diagram illustrating the structure of a standard cell. Each standard cell in a library is rectangular with a fixed height but varying widths. The cells are placed in rows with overlapping power supply paths. A standard cell typically has an N-well layer, an N-diffusion layer, a P-diffusion layer, a poly-silicon layer, a contact layer, and a metal-1 layer. The N-well, N-diffusion 330, P-diffusion and poly-silicon form P-MOS and N-MOS inside the cells. The poly-silicon also serves as an intra-cell routing path. The contacts 360 form connections between the routing layers and the under layers.

The height of a cell is typically given as the number of metal-1 tracks over the cells in the height direction. A metal-1 track comprises the metal-1 path and the space between metal-1 paths. The typical height of a standard cell is 10 tracks, where three tracks are used for power supply paths and the remaining seven tracks are for intra-cell design.

Placing features regularly in a direction facilitates the optimization of a lithography process in that direction and leads to a reduced feature size. In certain applications, the extra restrictions in layout increase the complexity of a design and might offset the benefits from the reduced critical dimension (CD). That means whether to apply the regular layout placement on one kind of features in a direction depends on how the CD of these features affects the cell area in that direction. Because MOSFETs in a standard cell are placed one by one in the width direction, such as those shown in Fig.1, the width of a cell is roughly determined by the product of the transistor pitch and the number of the transistors. Reduction of the contact size yields s a reduced transistor

pitch and leads to a decrease of the cell width. In one embodiment, it is the metal-1 pitch determines the height of a standard cell. The minimum pitch and size of contacts in the height direction is not critical for the height of standard cells. Applying a regular placement on the contacts in the height direction cannot help to decrease the height of a standard cell except for an increased difficulty in the layout compaction. Regularly-placed layout is applied on metal-1 layer to decrease the height. In one embodiment, multiple exposures are needed to fabricate the regularly-placed layout [WJ03]. The more layers on which regular placed layout is applied, the more extra masks and exposures are need. That may not be practical from an economics point of view [MF03].

Fig. 2a is a diagram showing the average contact pitch distribution of standard cells in the width direction. The dominant peak in the pitch distribution, which is one transistor pitch, should be used as the grid pitch in the width direction.

Fig. 2b is a diagram showing the average contact pitch distribution of standard cells in the height direction, there is no a dominant peak in the pitch distribution. That means the original placements of contacts are quite random in the height direction. Placing them regularly in the height direction increases the restriction during layout design and offsets some width decrease resulted from the regular placement in the width direction. Therefore, it would better to keep the height placement of contacts randomly.

Fig.3 is a layout of contacts for a demonstration of the invention. All contacts are placed randomly in the height direction while regularly in the width direction with ½ transistor pitch as the grid pitch.

Fig.4 illustrates the first step of the invention: an exposure of the reusable chromeless alternating phase-shifting template mask (Fig.4a) forms periodic dark lines on a wafer (Fig.4b). After the exposure, the opposite phase shift of patterns on the chromeless alternating phase-shifting template mask creates periodic unexposed dark lines at the boundary of 0° and 180° regions. The period of the 0° and 180° regions on the chromeless phase-shifting template mask is design to be one transistor pitch so that the period of the dark lines is half of that.

Fig.5 illustrates the second step of the invention: Exposures of the binary trim mask (Fig.5a) on the period dark lines which is formed by the exposure of the reusable chromeless alternating phase-shifting template mask. Fig.5b is the exposure image of the trim mask.

Fig.6 shows the final image of contacts by the overlap of the exposure of reusable template mask (Fig.4b) and the binary trim mask (Fig.5b). The Exposure of a binary trim mask on the periodic dark lines remove the unwanted parts of the dark lines and the small cuts of the dark lines left form the regularly-placed rectangular contacts. Like a short cut of a dark line, a contact in this method has different dimensions in different directions. The width size and location of contacts are determined by the width size and location of the dark lines, while the height dimension and position are determined by the size and location of the dark figures in the trim mask. Therefore, the width size of dark figures in a trim mask is not critical and can be made larger, while the height size of the dark figures in a trim mask is designed as small as possible according to the resolution of the exposure.

Because the features in the trim are placed randomly, the location of contacts in the height direction are also randomly.

Determined by the exposures of the different masks, the size of contacts is different in different directions. Using of regular placement and chromeless phase-shifting in the width direction, the size of contacts in the width direction is much smaller than the size of contacts in the height direction which is determined by the resolution of the exposure of the binary mask.

There are 2 masks (1 reusable template mask and 1 specific trim mask) and 2 exposures are needed to fabricate the rectangular regularly-placed contacts in standard cells. Since there is no extra specific mask needed comparing with the ordinary lithography method for randomly-placed contacts, the extra cost is kept to the lowest.

WHAT IS CLAIMED IS:

1. An optical lithography method to fabricate regularly-placed rectangular contacts in standard cells to decrease cell area and improve circuit performance.

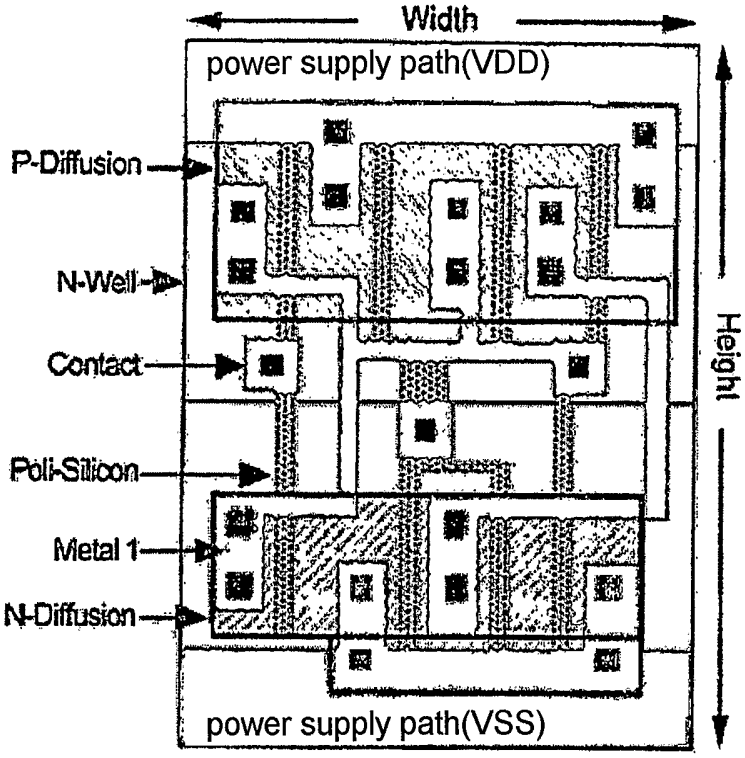


Fig.1 Typical layout of a standard cell

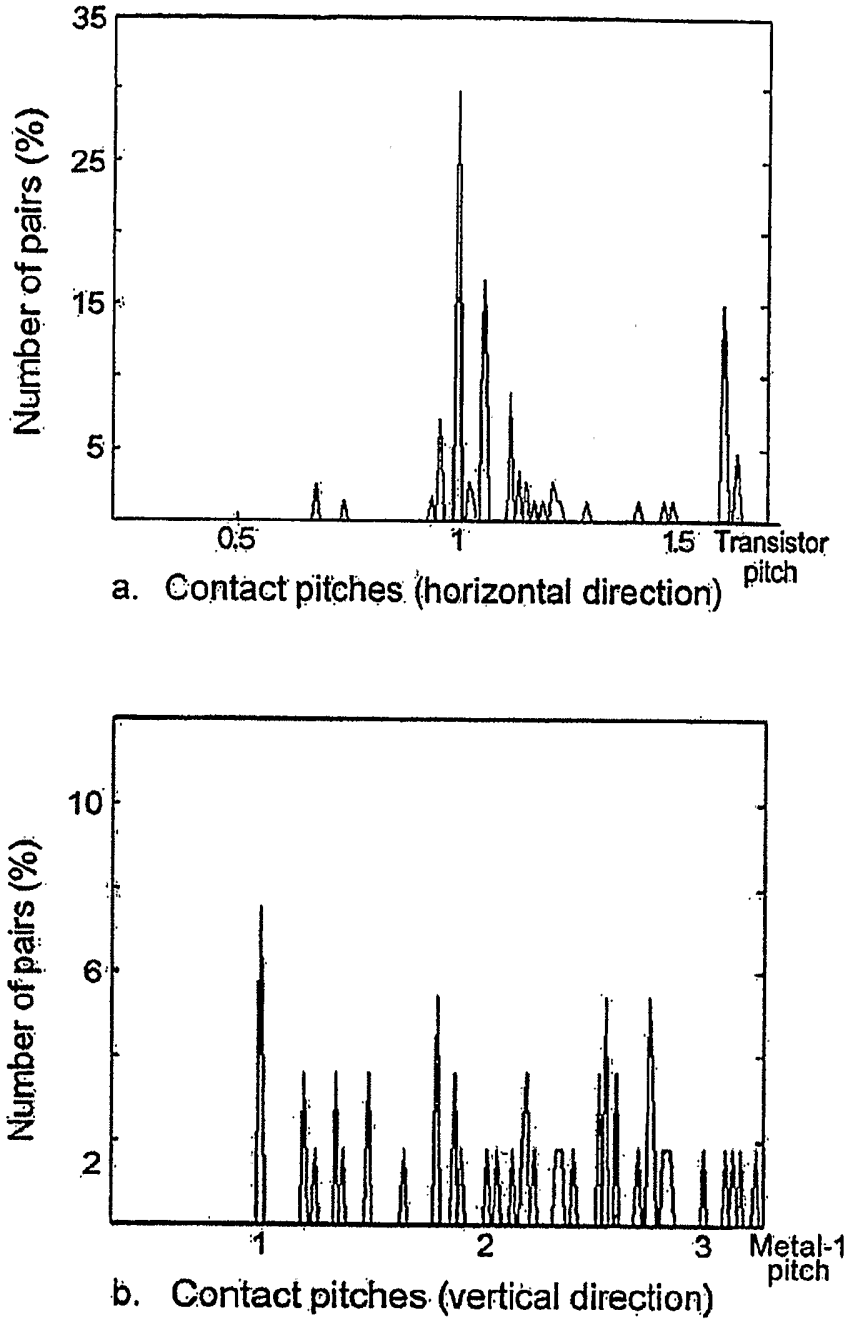


Fig.2 Average pitch distributions of contacts in standard cells in the two directions

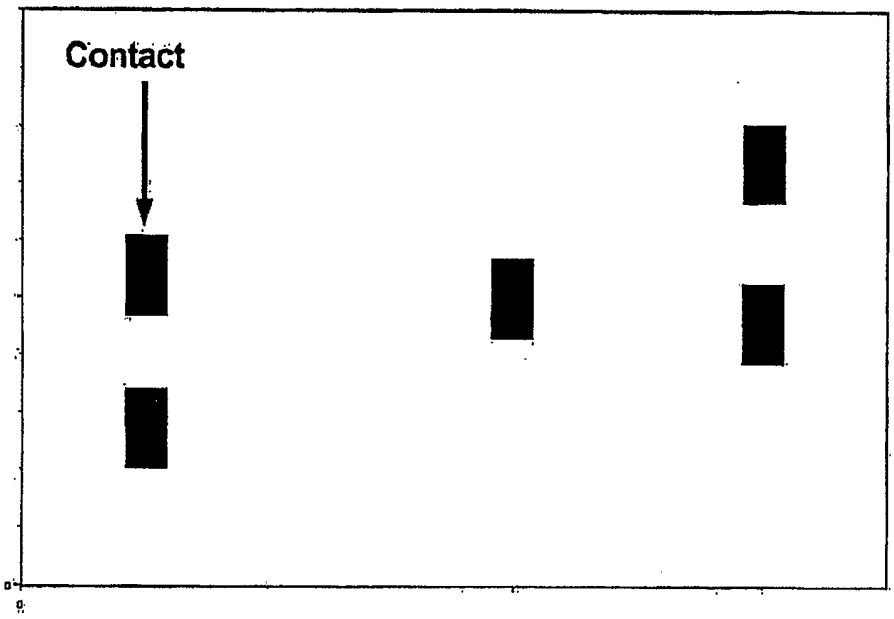
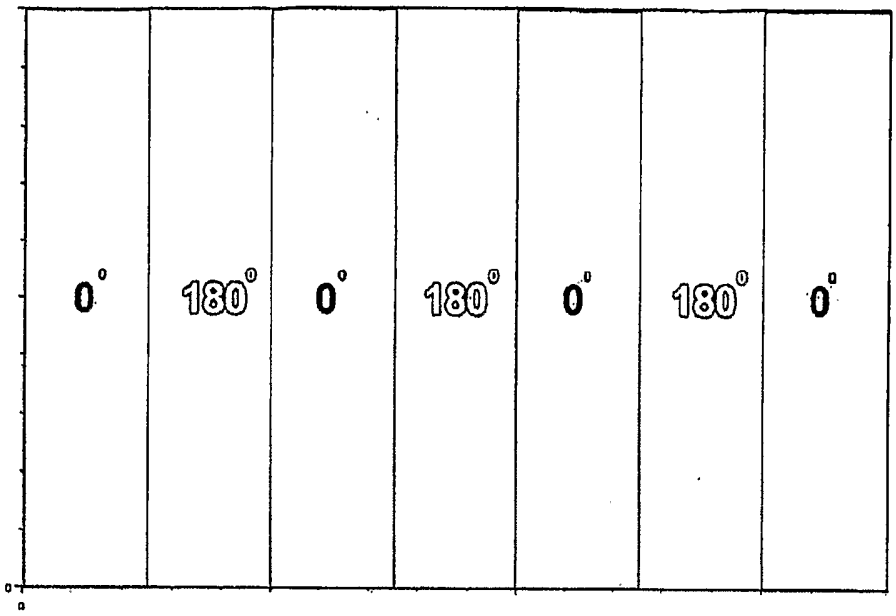
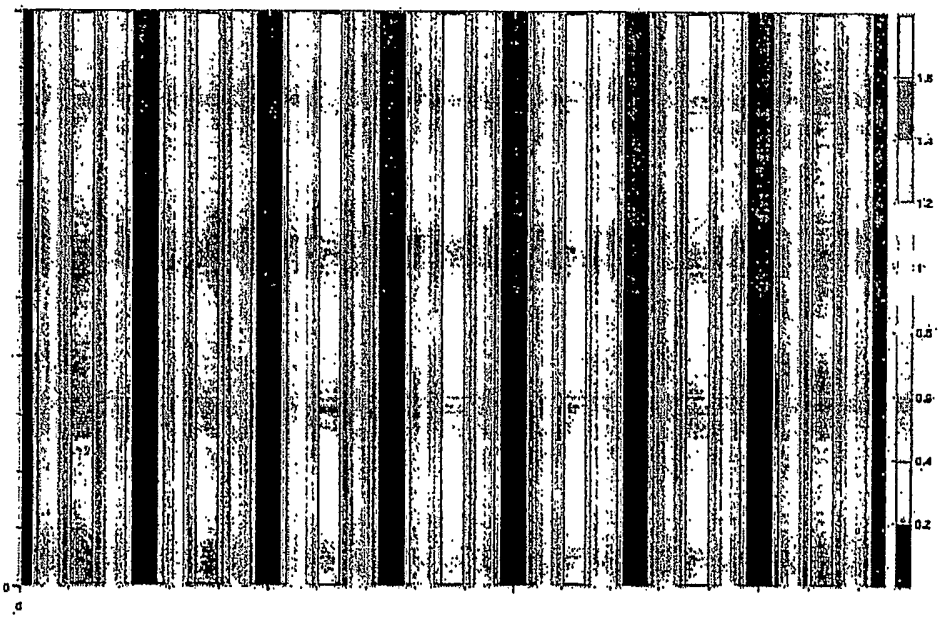


Fig.3 The demo layout of contacts.

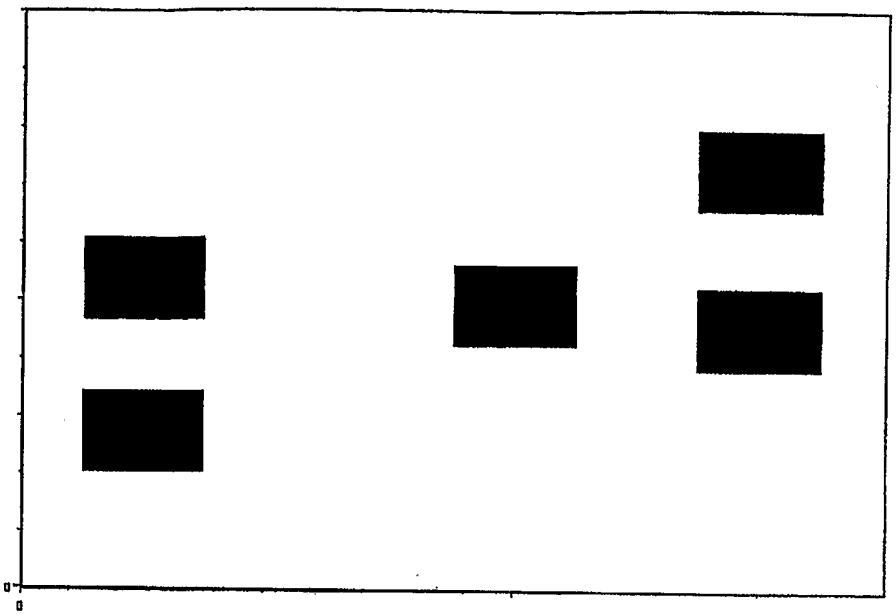


a. Chromeless alternating phase-shifting template mask for the second exposure

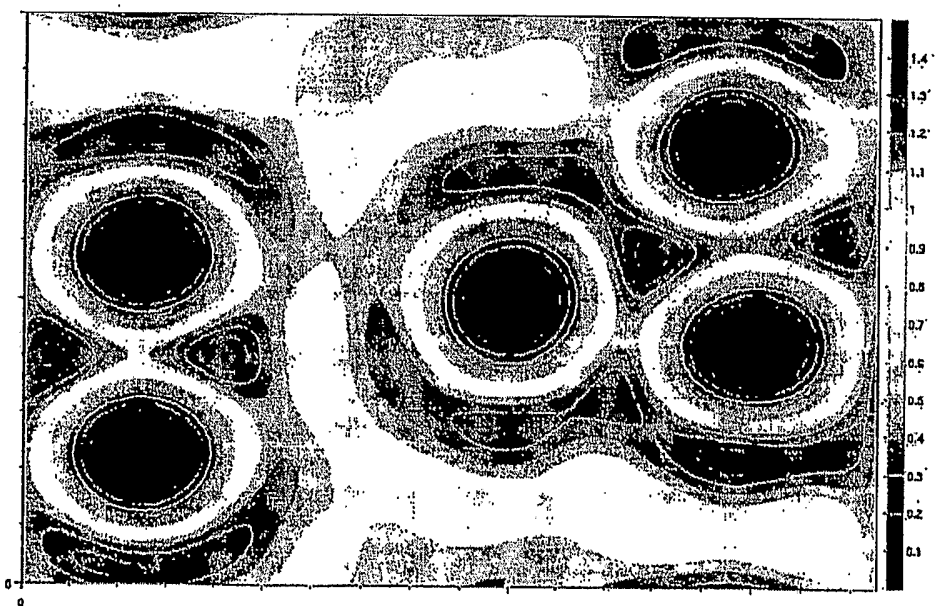


b. Exposure image of the template mask

Fig.4 The template mask and its expsoure image.



a. Binary trim mask of the demo contacts
for the second exposure



b. Exposure image of the binary trim mask for the demo contacts.

Fig.5 Trim mask and the exposure image of the test contacts

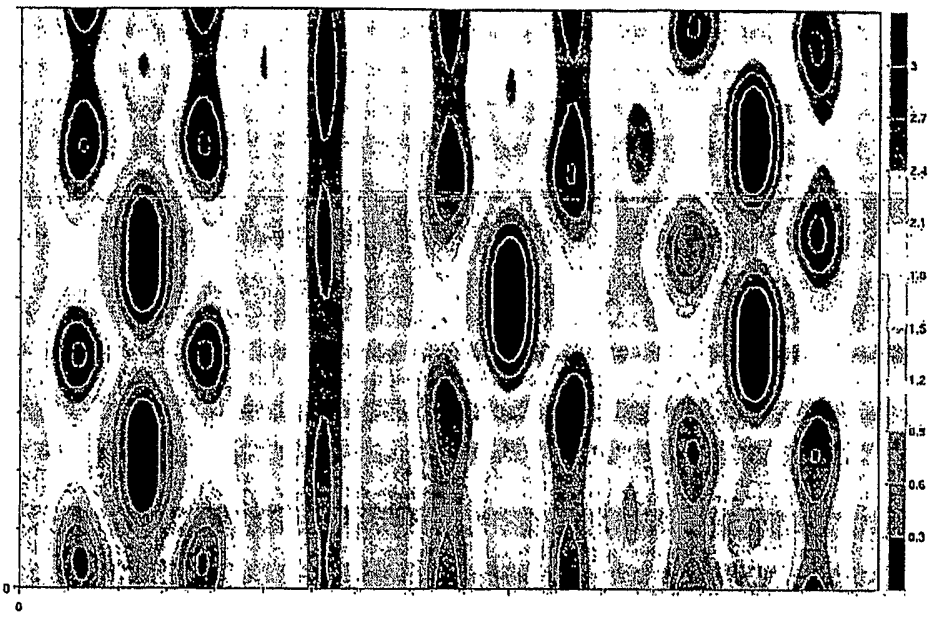


Fig.6 The overlap of the Fig.4b and the Fig.5b forms the final image of the demo contacts

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2005/000223

A. CLASSIFICATION OF SUBJECT MATTER

IPC[7] G03F 7/20 , H01L 21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[7] G03F 7/20 , G03F 7/213 , G03F 7/26 , G03F 7/16 , G03F 7/004 , G03F 7/00 , H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Chinese Invention, Chinese Utility Model

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, PAJ,EPODOC,CNPAT:optical , lithography , regular , cell , contact

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US-4456371(Burn J.Lin) 26.Jun.1984 (26.06.1984), (see the whole document)	1
X	US-A-6134008(Shuji) 17.Oct.2000 (17.10.2000), (see the whole document)	1
X	US-B1-6583041(Luigi) 24.Jun.2003 (24.06.2003), (see the whole document)	1

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

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"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19.Jun.2005 (19.06.05)	28 JUL 2005 (28.07.2005)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District 100088 Beijing, China Facsimile No. 86-10-62019451	Authorized officer Zhu, Ying Telephone No. 86-10-62085369

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US-4456371	26.Jun. 1984	EP-A1-0097831	11.Jan. 1984
		JP-A-59009922	19.Jan. 1984
		DE-G-3379080	2.Mar. 1989
US-A-6134008	17.Oct. 2000	JP-A-10032156	3.Feb. 1998
		US-A-5863677	26.Jan. 1999
US-B1-6583041	24.Jun. 2003	None	