(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 September 2003 (12.09.2003)

PCT

(10) International Publication Number
WO 03/075444 A1

(51) International Patent Classification[7]: H02M 7/00

(21) International Application Number: PCT/CN02/00920

(22) International Filing Date:
30 December 2002 (30.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/086,688 4 March 2002 (04.03.2002) US

(71) Applicant: **THE UNIVERSITY OF HONG KONG** [CN/CN]; G18, Eliot Hall, Pokfulam Road, Hong Kong (CN).

(72) Inventors: **POON, Ngaikit, Franki**; 1st Floor, 312 Kilung Street, Sham Shui Po, Kowloon, Hong Kong (CN). **PONG, Manhay**; Flat, G, 1st Floor, Tower 13A, Yee Fai Court, South Horizons, Ap Lei Chau, Hong Kong (CN). **LIU, Chuipong, Joe**; Flat 3406, Kwai Fung House, Kwai Chung, New Territories, Hong Kong (CN).

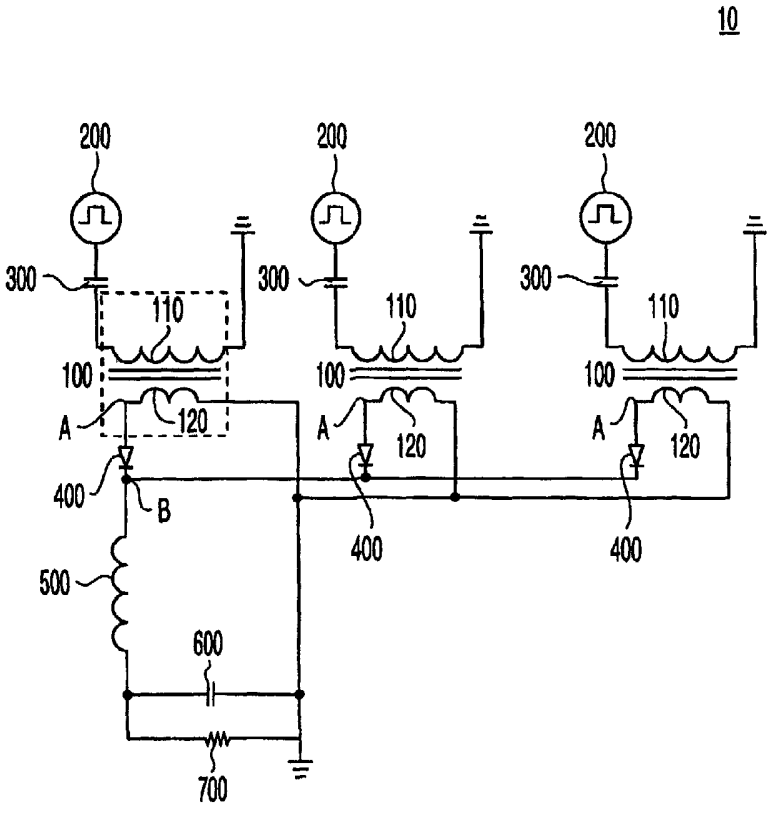
(74) Agent: **CHINA PATENT AGENT (H.K.) LTD.**; 22/F, Great Eagle Centre, 23 Harbour Road, Wanchai, Hong Kong (CN).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),

[Continued on next page]

(54) Title: AC-DC CONVERTER WITH LOW RIPPLE OUTPUT



(57) Abstract: An AC-DC converter that includes a plurality of power conversion units that overlay their signals to generate a DC signal with low voltage level, small voltage and current ripples, but high DC current. The DC signal is further filtered by a LC low pass filter to further minimize the ripples before output to the load. In one embodiment, the plurality of power conversion units is preferably powered by a plurality of input pulse generators. In an alternative embodiment, the power conversion units is powered by a input pulse generator circuit that includes a plurality of n-channel MOSFETs arranged in a full bridge configuration whose gate voltages are controlled by a plurality of pulse generators.

WO 03/075444 A1

Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

AC-DC CONVERTER WITH LOW RIPPLE OUTPUT

FIELD OF THE INVENTION

The present invention relates generally to an AC-DC converter and, more specifically, to an AC-DC converter that produces a DC signal with small ripples.

BACKGROUND

FIG. 1A illustrates a typical AC-DC converter, which includes a power conversion unit, an inductor-capacitor low-pass filter, and an input pulse generator. The power conversion unit includes a transformer with a primary and a secondary winding and two rectifier diodes with their anodes coupled to either prongs of the secondary winding respectively. The cathodes of the diodes are, in turn, connected to each other as well as to the low-pass filter. The primary winding is connected to the input pulse generator.

In operation, the input pulse generator outputs an AC signal, illustrated in FIG. 1B, across the primary winding. The signal across the primary winding is then transferred to the secondary winding, where negative portion of the signal is rectified by the rectifying diodes to yield the signal illustrated in FIG. 1C. This signal is then filtered by the low-pass filter to output a DC output signal that includes output ripples, as depicted in FIG. 1E.

Although output ripples are only small perturbations when output DC voltage level is high, the ripples become a prominent feature when the output DC voltage level is low. Since a variety of modern semiconductor devices such as microprocessors typically operate at low DC voltage levels, the ripples may interfere with the proper operation of the devices. Typical modern semiconductor devices have a tolerable ripple limit of about 1% of the DC voltage. Voltage ripple is of increased concern for semiconductor devices that operate at lower DC voltages, for example 1 V, because the absolute tolerable ripple decreases as the operating voltage decreases.

One way to minimize output ripples is by improving filtering capabilities of the converter. This may be achieved by increasing the capacitance and/or lowering the impedance of the capacitor in the low-pass filter. Real capacitors having a low series impedance or typically

expensive. However, large capacitors take up more space and low impedance capacitors are expensive. Alternatively, a larger inductor may be used to improve filtering capabilities. However, a larger inductor also takes up more space. In addition, they saturate much easier.

Another way to reduce output ripples is to increase the frequency of the input signal. However, high frequency current flowing through the inductor produces high frequency flux change in the inductor ferrite, which increases core loss and decreases efficiency of the inductor. In addition, inductors with low loss ferrite material is expensive.

Some work has been done to reduce output ripples by modifying the typical AC-DC converter circuit. For example, US patent 5,668,464 to Krein *et al.*, which is incorporated herein, claims an AC-DC converter circuit that incorporates a feedback control circuit that generates an AC ripple signal to cancel out output ripples. Drawbacks of this converter circuit are that the feedback control circuit not only adds complexity to the circuit but also takes up precious space within small semiconductor devices. In addition, the output inductor carries large AC current ripples that can degrade the inductor. Another patent, US Patent 5,663,876 to Newton *et al.*, which is incorporated herein, describes a rectifier circuit with two output inductors that can produce a DC signal without any output ripples. However, this can only be achieved by using inductors with specific inductance values operating at a predetermined operating condition. In addition, current and voltage ripples across the two output inductors are large and can degrading their performance.

Therefore, there is a need for an improved AC-DC converter that produces a DC signal with low DC voltage level, small voltage and current ripples, but high DC output current without large capacitors and/or inductors, addition of complex circuits, or strict operating requirements.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an AC-DC converter that produces a DC signal with low voltage level and small output ripples without large capacitors and/or inductors, addition of complex circuits, or strict operating requirements.

It is another object of the present invention to provide an AC-DC converter that produces a DC signal with low voltage level, small voltage and current ripples across the output inductor, but high DC output current without large capacitors and/or inductors, addition of complex circuits, or strict operating requirements.

Briefly, the present invention provides an AC-DC converter that includes a plurality of power conversion units that overlay their signals to generate a DC signal with low voltage level, small voltage and current ripples, but high DC current. In a preferred embodiment, the AC-DC converter comprises a plurality of power conversion units, an input pulse generator system, and a low pass filter. Each power conversion unit preferably includes a transformer with a primary and a secondary winding, a DC blocking capacitor connected to the primary winding, and a rectifier diode with its anode connected to the secondary winding. The cathodes of the rectifier diodes are connected to one another as well as to the low pass filter, thereby connecting each power conversion unit to each other as well as to the low pass filter. The low pass filter is preferably an inductor-capacitor low pass filter. The input pulse generator system preferably includes a plurality of input pulse generators, each connected to the DC blocking capacitor of a power conversion unit.

In operation, each input pulse generator preferably outputs a square wave input signal that is the same as but out of phase with signals generated by other generators, so that the signals overlap and at least one of the signals is high at any given moment. In one embodiment, the square wave signals are evenly phase-shifted with respect to one another. Each input signal is transmitted to a primary winding through a DC blocking capacitor, which filters away any DC biases in the signal, and is then transferred from the primary winding to the secondary winding. The signal at each secondary winding is then transmitted to a rectifying diode, which rectifies the negative portion of the signal. Each rectified signal is then overlaid to generate a DC signal with low DC voltage level, small voltage and current ripples, but high DC current. The DC signal is then filtered by the low pass filter to further reduce voltage and current ripples to generate the DC output signal.

In an alternative embodiment, the AC-DC converter includes the same power conversion unit and low pass filter as the converter described above but with a modified input pulse generator

system. The modified input pulse generator system preferably includes a first, second, third, and fourth n-channel MOSFET arranged in a full bridge configuration, where the drains of the first and third MOSFET are connected to each other and to ground, the sources of the same MOSFETs are connected to the drains of the second and fourth MOSFET respectively, and the sources of the second and fourth MOSFETs are connected to a DC voltage source and a DC blocking capacitor. The DC blocking capacitor is also connected to a first and second power conversion unit, where the first and second primary winding of the first and second power conversion unit each connect to the DC blocking capacitor on one prong and to the sources of the first and third MOSFET respectively on the other prong. Preferably, a first, second, third, and fourth pulse generator are connected to the gate of the first, second, third, and fourth MOSFET respectively. The first and second pulse generators output square pulses to alternately switch the first and second MOSFETs on; that is, either the first or the second MOSFET is switched on, but never at the same time. A brief period during which both MOSFETs are switched off is inserted in between alternately switching of the MOSFETs to prevent connecting the DC voltage source to ground. By alternately switching the first and second MOSFET on, the first primary winding is alternately connected to the DC voltage source and ground, generating a signal across the winding.

The third and fourth pulse generators output the same signals as the first and second pulse generators respectively but phase-shifted by 180 degrees. This generates a signal across the second primary winding that is the same signal as that across the first primary winding but phase-shifted by 180 degrees. The signals across the first and second primary winding preferably stay high longer than they are low, so that the two signals overlap while they are high and at least one signal is high at any one moment. The signals at the primary windings are then transferred to the secondary windings and then to the rectifying diodes, where negative portions of the signals are rectified. The rectified signals are then overlaid to create a DC signal with low voltage level with small voltage and current ripples but high DC current. The overlaid DC signal is then filtered by the inductor-capacitor low pass filter to further minimize ripples before output to a load.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic diagram of a typical prior art AC-DC converter;

FIG. 1B is a graph of the input signal generated by the input pulse generator across the primary winding of the converter depicted in FIG. 1A;

FIG. 1C is a graph of the signal depicted in FIG. 1B after it is transferred from the primary winding to the secondary winding and is rectified by rectifying diodes of the converter depicted in FIG. 1A;

FIG. 1D is a graph of the current that flows through the inductor of the converter depicted in FIG. 1A;

FIG. 1E is a graph of the output DC signal of the converter depicted in FIG. 1A;

FIG. 2 is a schematic diagram of a preferred AC-DC converter according to the invention;

FIGs. 3A-C are graphs of signals generated by input pulse generators of the converter depicted in FIG. 2;

FIGs. 3D-F are graphs of signals across the secondary windings of the converter depicted in FIG. 2;

FIG. 3G is a graph of the signal at node B of the converter depicted in FIG. 2;

FIG. 3H is a graph of the current across the output inductor of the converter depicted in FIG. 2;

FIG. 3I is a graph of the output DC signal of the converter depicted in FIG. 2;

FIG. 4 is an alternative embodiment of the AC-DC converter according to the invention;

FIGs. 5 A-D are graphs of signals generated by pulse generators of the converter depicted in FIG. 4;

FIGs. 5E-F are graphs of signals across the secondary windings of the converter depicted in FIG. 4;

FIG. 5G is a graph of the signal at node B of the converter depicted in FIG. 4;

FIG. 5H is a graph of the current across the output inductor of the converter depicted in FIG. 4; and

FIG. 5I is a graph of the output DC signal of the converter depicted in FIG. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 2 illustrates a preferred embodiment of an AC-DC converter 10 in accordance with the present invention. As shown in FIG. 2, AC-DC converter 10 preferably includes a plurality of power conversion units that each includes a transformer 100 with primary winding 110 and secondary winding 120, a DC blocking capacitor 300 connected to primary winding 110, and a

rectifier, such as a rectifier diode 400 connected to secondary winding 120. It should be understood that the transformers may be replaced with inductors for non-isolation of AC-DC converter 10.

Upon reference to the present specification, one of ordinary skill in the art would understand that although three power conversion units are depicted in FIG. 2, fewer or additional units may be added with proper modifications. Increasing the number of power conversion units preferably decreases the relative amount of ripple present in the DC output voltage. More power conversion units may be added to any embodiment of the invention to decrease voltage ripple and increase DC current output.

An input pulse generator 200 is connected to each DC blocking capacitor 300. The cathodes of diodes 400 are preferably connect at node B so that signals from each power conversion unit are channeled to and overlaid at the node. Overlaying signals from a plurality power conversion units advantageously provides a DC signal with low voltage level, small voltage and current ripples, but high DC current, as discussed below in conjunction with FIG. 3G. An inductor-capacitor (LC) low-pass filter formed by inductor 500 and capacitor 600 connects to the cathodes of rectifying diodes 400 at node B. The output prong of inductor 500 of the LC low-pass filter supplies the output DC signal to load 700.

Various aspects of the operation of AC-DC converter 10 are depicted in FIGs. 3A-H. FIGs. 3A-C, illustrate signals generated by input pulse generators 200. Each input pulse generator 200 preferably provides a time-varying electrical signal. Thus, input pulse generators 200 generate preferably periodic waveforms such as square waves of preferably equal magnitude and pulse width that are staggered evenly in time, so that, at any one moment, at least one of the input signals is high. That is, the time-varying electrical signals provided by input pulse generators 200 are out of phase.

The waveforms output by pulse generators may have a constant or varying frequency. A non-limiting range of suitable frequencies would include for example frequencies in the range of about 25 kHz to about 1 mHz, such as from about 100 kHz to about 500 kHz. Upon reference to the present specification, one of ordinary skill in the art would understand that the values, such as the capacitance and inductance, of the components of AC-DC converter 10 depend upon the frequencies of the waveforms received from the pulse generators.

Each input signal is transmitted to a primary winding 110 through a DC blocking capacitor 300, which reduces and preferably blocks any DC bias in the signal to prevent saturation of

transformers 100. Each signal is then transferred from primary winding 110 to secondary winding 120, which transfer prepares time-varying output signals.

The time-varying output signals at secondary windings 120 (node A) are illustrated in FIGs. 3D-F. These signals are shaped by impedances of capacitors 300 and primary windings 110 resulting in sawtooth-like waveforms that are slightly voltage-shifted downwards. The time-varying signals at the secondary windings 120 have a smaller absolute DC bias than the input signals accepted by AC-DC converter 10. By absolute DC bias, it is meant the absolute value of the DC bias.

The time-varying output signals at secondary windings 120 (node A) are rectified by diodes 400 so that only the positive portions of the signals remain. After rectification, signals from each power conversion unit are channeled to and overlaid together at node B to result in the signal depicted in FIG. 3G. As can be seen in the figure, before a signal from one power conversion unit can decay to any significant extent, a second signal from another power conversion unit is overlaid on top of the first signal, resulting in a DC signal with minimum voltage and current ripples. In addition, overlaying of signals allows each power conversion unit to contribute to the total current at node B, increasing current level of the signal at the node and at the converter output. The rectifiers may be reversed to obtain a negative DC output voltage.

In an alternative embodiment, rectifying diodes 400 may be replaced with electronic switches, such as, for example, MOSFET or synchronous rectifiers. A synchronous rectifier is provided by replacing a diode with a MOSFET. For example, diode 400 may be replaced by a MOSFET having a proper gate driving sequence. The gate driving voltage of the MOSFET is programmed to turn on when the circuit path, in which the MOSFET is located, is under forward current. A MOSFET may have a voltage drop of less than about 0.6 V, which voltage is typical of diodes.

Returning to FIGs 3A-3I, the signal at node B is next filtered by a LC low-pass filter formed by inductor 500 and capacitor 600 to further reduce voltage and current ripples, yielding an output DC signal depicted in FIG. 3I. Besides serving as a filtering element for minimizing ripples, inductor 500 also acts as a defined equivalent DC current source for load 700 with current equal to the DC output current of AC-DC converter 10. With a defined current load, input pulse generators 200 would be able to generate input current waveforms in phase with input pulse signals. In addition, a defined current source load minimizes numerous undesired

circuit behavior such as resonance between leakage inductance of the transformer or undefined capacitance on the load side. A defined current source load also draws smaller a RMS current from diodes 400 and input pulse generators 200, thereby reducing signal loss caused by current peak. Diodes 400 or pulse generators 200 preferably experience a square-wave like current waveform, which provides a minimum RMS value as compared to the average value of the current. The waveform shape is determined a square wave by the inductor rather than by the unpredictable load current. The average value of the current is determined by the load.

Referring to Fig. 3G, the voltage ripple at B does not go to zero as it does in prior art voltage supplies where the voltage ripple at the output inductor is a switching square wave. Because the ripple at B is small, output inductor 500 does not require a large inductance. Preferably, the inductance of inductor 500 is selected to provide a defined current source load to pulse generators 200 and diodes 400. Because output inductor 500 is much smaller than prior art filter inductor, a suitable inductor may be parasitic inductance from the circuit such as printed circuit board trace inductance.

The magnitude of the output voltage is determined by the amplitude of the input pulses, the duty cycle of the pulse width, and the turn ratio of the isolation transformers. For example, an increase in the amplitude of the input pulses would increase the amplitude of the DC output voltage, as would a decrease in the turn ratio of the isolation transformers. Here, the turn ratio is defined as Nprimary/Nsecondary, where N is the number of turns of the primary and secondary windings. As the number of secondary turns, Nsecondary, increases, the turn ratio will decrease, thereby increasing the output voltage.

An AC voltage waveform, such as a square wave, applied to a transformer preferably has a DC component of zero. For a voltage waveform having a zero DC component, the positive area under a voltage v time curve of the waveform is equal to the absolute value of the negative area under the voltage v time curve. That is, the integral of the positive area of the waveform is equal to the absolute value of the integral of the negative area. When the duty cycle of the input pulses is varied, the AC voltage produced by the transformer preferably varies in such a way as to provide a constant voltage time integral. By constant time integral, it is meant that the integral of the positive area remains equal to the absolute value of the negative area of the waveform. Additionally, it is preferred that the peak to peak voltage of the waveform also remains constant as the duty cycle varies. For example, if the absolute

value of the peak negative amplitude decreases, the peak positive amplitude preferably increases to maintain a constant peak to peak voltage. This produces variation of the positive amplitude after rectification and, thus, the DC output voltage.

AC-DC converter 10 according to the invention can be modified into an AC-DC converter 20 illustrated in FIG. 4. The modified AC-DC converter includes an input pulse generator circuit, two power conversion units, and a capacitor-inductor low pass filter. The input pulse generator circuit preferably accepts a plurality of input signals from pulse generators 230 to thereby prepare intermediate time-varying signals applied to the power conversion units. The power conversion units output time-varying signals that are combined to prepare a direct current output signal.

The input pulse generator circuit includes a plurality of field effect transistors, such as four n-channel MOSFETs 210A-D, DC voltage source 240, and pulse generators 230 A-D. N-channel MOSFETs 210 A-D are arranged in a full bridge configuration with drains of MOSFETs 210 A and C coupled to a DC voltage source 240 and their sources coupled to the drains of MOSFETs 210 B and D, respectively. The sources of MOSFETs 210 B and D are coupled to ground and DC blocking capacitor 300. Each gate of MOSFETs 210 A-D is coupled to a pulse generator 230 A-D that are each programmed to output pulses of specific period and amplitude as described in conjunction with FIGs. 5A-D below. The MOSFETs preferably operate as switches toggling between the on and off states as described below. Thus, p-channel MOSFETs, which may also be used to perform a switching function, may be used in an AC-DC converter of the invention.

Input signal generator circuit supplies input signals to two power conversion units. Each power conversion unit includes a transformer 100 and a rectifying diode 400. The two power conversion units also share one DC blocking capacitor 300, eliminating the need for additional capacitors. Primary windings 110 A and B are coupled to nodes C and D, respectively, and to DC blocking capacitor 300. Secondary windings 120 are each coupled to diodes 400. The cathodes of diodes 400 are connected to node B so that signals from each power conversion unit are channeled to and overlaid at the node. Node B is, in turn, connected to a LC low-pass filter formed by inductor 500 and capacitor 600. The output prong of inductor 500 of the LC low-pass filter outputs the resultant DC signal to load 700. It should be understood that the transformers may be replaced with inductors for non-isolation of AC-DC converter 20.

Various aspects of the operation of AC-DC converter 20 are illustrated in FIGs. 5A-I. The first four figures, FIGs. 5A-D, depict signals generated by pulse generators 230 that are applied to gates of MOSFETs 210A-D. Signals from pulse generators 230A and 230C are identical but phase shifted by 180 degrees. Similarly, signals from pulse generators 230B and 230D are also identical but phase shifted by 180 degrees. Timing of the pulses is crucial for minimizing ripples in the DC output of AC-DC converter 10, as discussed below in conjunction with FIG. 5G.

When the signal at pulse generator 230A is high and the signal at pulse generator 230B is low, MOSFET 210A is switched on while MOSFET 210B is switched off, connecting primary windings 110A to DC voltage source 240 at node C. With capacitor 300 at a lower potential than DC voltage source 240, a potential drop is established across primary winding 110A, causing current to flow across primary winding 110 A to charge capacitor 300. As capacitor 300 charges, the potential difference across primary winding 110 A decreases.

When the signal at pulse generator 230A is low and the signal at pulse generator 230B is high, MOSFET 210A is switched off and MOSFET 210B is switched on, connecting primary winding 110 A to ground through node C. The voltage difference across primary winding 110 A is now reversed, with capacitor 300 discharging voltage and current through primary winding 110 A to ground through point C. As capacitor 300 discharges, the voltage difference across primary winding 110 A decreases.

A brief period during which signals from both pulse generators 230 A and B are low is inserted between alternately switching MOSFETs 210A and B so that the MOSFETs are never switched on simultaneously. Thus, for example, waveforms 5A-5B and 5C-5D represent first and second pairs of preferably orthogonal waveforms. This prevents connecting DC voltage source directly to ground and damaging the DC voltage source. When signals 230A and 230B are low, the waveform across the primary winding 110A will be either positive or negative depending upon the magnetizing current of the primary winding. The magnetizing current of the primary winding will flow through the body diodes of two diagonal MOSFETs. The body diodes are inherent to each MOSFET and connected in antiparallel therewith. The direction and magnitude of the magnetizing current depends upon the magnetizing inductance, operating duty cycle and the phase of the transformer. Preferably, the time period is small and will prevent the preparation of a low output ripple voltage.

The interoperation of pulse generators 230 A and B with MOSFETs 210 A and B creates a

saw-tooth like waveform shifted downwards across primary winding 110 A as illustrated in FIG. 5E. The general shape of the waveforms is caused by the charging and discharging of capacitor 300 as well as the impedances of MOSFETs 210 A and B and primary winding 110A. Input pulse generators 230 C and D and MOSFETs 210 C and D interoperate in the same manner as input pulse generators 230 A and B and MOSFETs 210 A and B but phase shifted by 180 degrees to generate the waveform illustrated in FIG. 5F across primary winding 110 B.

The sharing of the DC blocking capacitor 300 is an advantage of AC-DC converter 50. For example, in the event that the DC blocking capacitor is being charged through winding 110 A and being discharged by winding 110B, the RMS current flowing through the blocking capacitor is preferably reduced. Thus, as compared to other voltage sources, a smaller or lower quality capacitor may be used.

Signals are passed from primary windings 110 to secondary windings 120 where they are rectified by diodes 400 so that only the positive portions of the signals remain. Signals from each power conversion units are then overlaid at node B resulting in the signal depicted in FIG. 5 G. Specifically, before a first signal from one power conversion unit can decay to any significant extent, a second signal from a second power conversion unit is overlaid on top of the first signal, resulting in a DC signal with minimum voltage and current ripples at node B as well as at the converter output. Overlaying of signals from a plurality of power conversion units also allows each power conversion unit to contribute current at node B, increasing current level of the signal at the node and, thus, at the converter output. The signal at node B is further filtered by a LC low-pass filter formed by inductor 500 and capacitor 600 to further reduce voltage ripples, yielding a DC signal depicted in FIG. 5I. The rectifiers may be reversed to obtain a negative DC output voltage.

The amplitude of the DC output voltage is determined by the duty cycle of the pulses generated by pulse generator 230. Increasing the on duty cycle increases the average DC voltage of the pulse generators and, hence, increase the voltage across the DC blocking capacitor. With a higher voltage across the DC blocking capacitor 300, the potential difference across primary windings 110A and B is smaller when primary windings 110 A and B are connected to DC voltage source 240, decreasing the amplitude of the signal at node B and, thus at the output.

AC DC converter 10 or 20 may be modified to eliminate sharp voltage edges and undesired

voltage spikes caused by parasitic or leakage impedance in transformers 100 or other circuit elements. For example, snubber circuits may be added across rectifying diodes 400, secondary winding 120, or across low pass filter 500 and 600.

The present invention is not to be limited in scope by the specific embodiments described herein, which are intended as single illustrations of individual aspects of the invention, and functionally equivalent methods and components are within the scope of the invention. Indeed, various modifications of the invention, in addition to those shown and described herein will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Such modifications are intended to fall within the scope of the appended claims.

All publications and patent applications mentioned in this specification are herein incorporated by reference to the same extent as if each individual publication or patent application was specifically and individually indicated to be incorporated by reference.

What Is Claimed Is:

1.A device for preparing a direct current (DC) signal from a plurality of input signals, comprising:

a plurality of power converters, each power converter configured to prepare a time-varying output signal from a respective input signal, each time-varying output signal having a respective, different phase; and

an overlaying circuit for combining the time-varying output signals to thereby prepare the DC signal.

2.The device of claim 1, wherein each power converter comprises a capacitor connected to a transformer, wherein the capacitor accepts the input signal and the transformer outputs the time-varying output signal.

3.The device of claim 1, wherein the overlaying circuit comprises a plurality of rectifiers to rectify the time-varying output signals.

4.The device of claim 3, wherein the overlaying circuit combines the time-varying output signals after rectification.

5.The device of claim 3, wherein the rectifiers are diodes.

6.The device of claim 1, wherein each input signal is a time-varying input signal having a respective different phase.

7.The device of claim 6, wherein each input signal comprises at least one of a square wave and a sinusoid.

8.The device of claim 6, further comprising at least one power source to provide the plurality of input signals.

9. The device of claim 6, wherein an absolute DC bias of the time-varying output signals is

less than an absolute DC bias of the time-varying input signals.

10. A device for preparing a direct current (DC) signal from a plurality of input signals, comprising:

an input circuit for preparing a plurality of intermediate time-varying signals from the plurality of input signals;

a plurality of power converters, each power converter configured to prepare a time-varying output signal from a respective intermediate time-varying signal, each time-varying output signal having a respective, different phase; and

an overlaying circuit for combining the time-varying output signals to thereby prepare the DC signal.

11. The device of claim 10, wherein the input circuit comprises first and second sets of transistors, each member of the first and second sets having a respective drain, source, and gate.

12. The device of claim 11, wherein the transistors are metal-oxide semiconductor field effect transistors (MOSFETs).

13. The device of claim 12, wherein the drain of each member of the first set of transistors is biased at a DC voltage and the source of each member of the first set of transistors is in electrical communication with a respective power converter.

14. The device of claim 13, wherein the drain of each member of the second set of transistors is in electrical communication with a source of a respective member of the first set of transistors.

15. The device of claim 14, wherein the gate of each member of the first and second sets of transistors accepts a respective one of the input signals, the input signals accepted by the first and second sets of transistors having a different duty cycle.

16. The device of claim 15, wherein the gate of each member of the first and second sets of

transistors accepts a respective one of the input signals, the input signals accepted by the first and second sets of transistors having a different phase.

17. The device in accordance with claim 10, wherein said input circuit comprises a plurality of MOSFETs connected in a full-bridge configuration.

18. The device in accordance with claim 17, wherein said input circuit further comprises a DC voltage source connected to a drain of each member of a subset of the MOSFETs.

19. The device accordance with claim 18, wherein a respective input signal from a power source controls a gate voltage of each of said plurality of MOSFETs to thereby prepare the intermediate time-varying signals.

20. The device according to claim 19, wherein each input signal is a time-varying input signal.

21. The device in accordance with claim 20, wherein said input signals switch MOSFETs on and off by controlling gate voltages of said MOSFETs so as to alternatively connect said power converters to a DC voltage source or ground.

22. The device in accordance with claim 21, wherein each power converter comprises a transformer with a primary and a secondary winding.

23. The device according to claim 22, wherein each said power converter further comprises a rectifying diode whose anode connects to said secondary winding and whose cathode connects to cathode of at least one other rectifying diode of another said power converter.

24. The device according to claim 10, wherein the input signals comprise first and second pairs of orthogonal time varying electrical signals.

25. A method for preparing a direct current (DC) signal from a plurality of input signals, comprising:

preparing a plurality of time-varying output signals from the input signals, each of the time-varying output signal having a respective, different phase; and

combining the time-varying output signals to thereby prepare the DC signal.

26. The method of claim 25, wherein the step of combining further comprises rectifying the time-varying output signals.

27. The method of claim 26, wherein the time-varying output signals are rectified prior to combining.

28. The method of claim 25, wherein the step of preparing the time-varying output signals further comprises reducing a DC bias of the input signals.

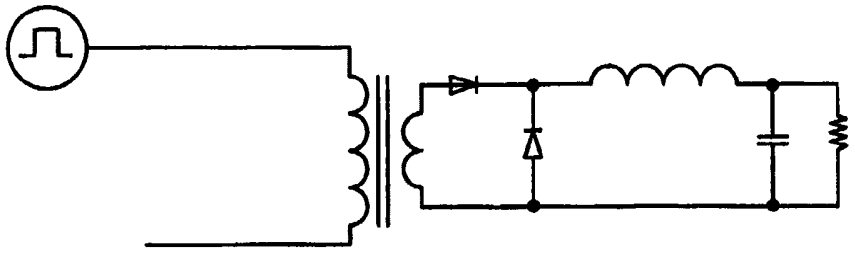


FIG. 1A
(Prior Art)

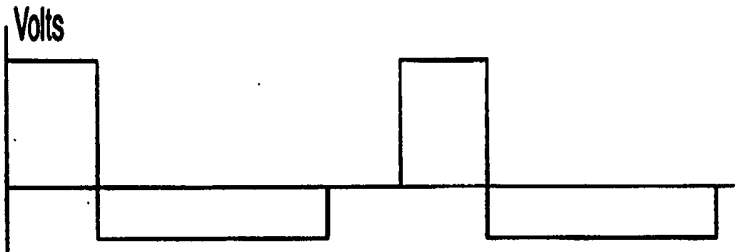


FIG. 1B

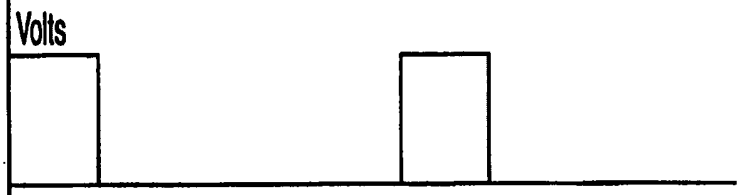


FIG. 1C

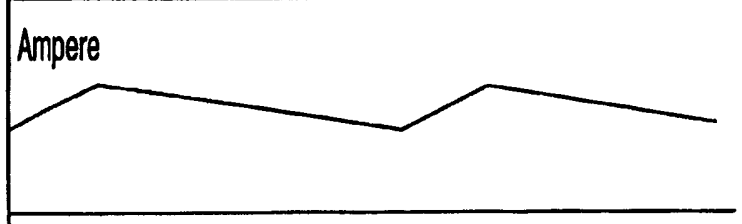


FIG. 1D

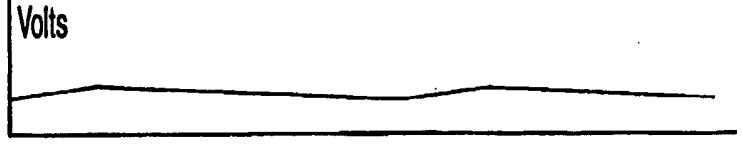


FIG. 1E

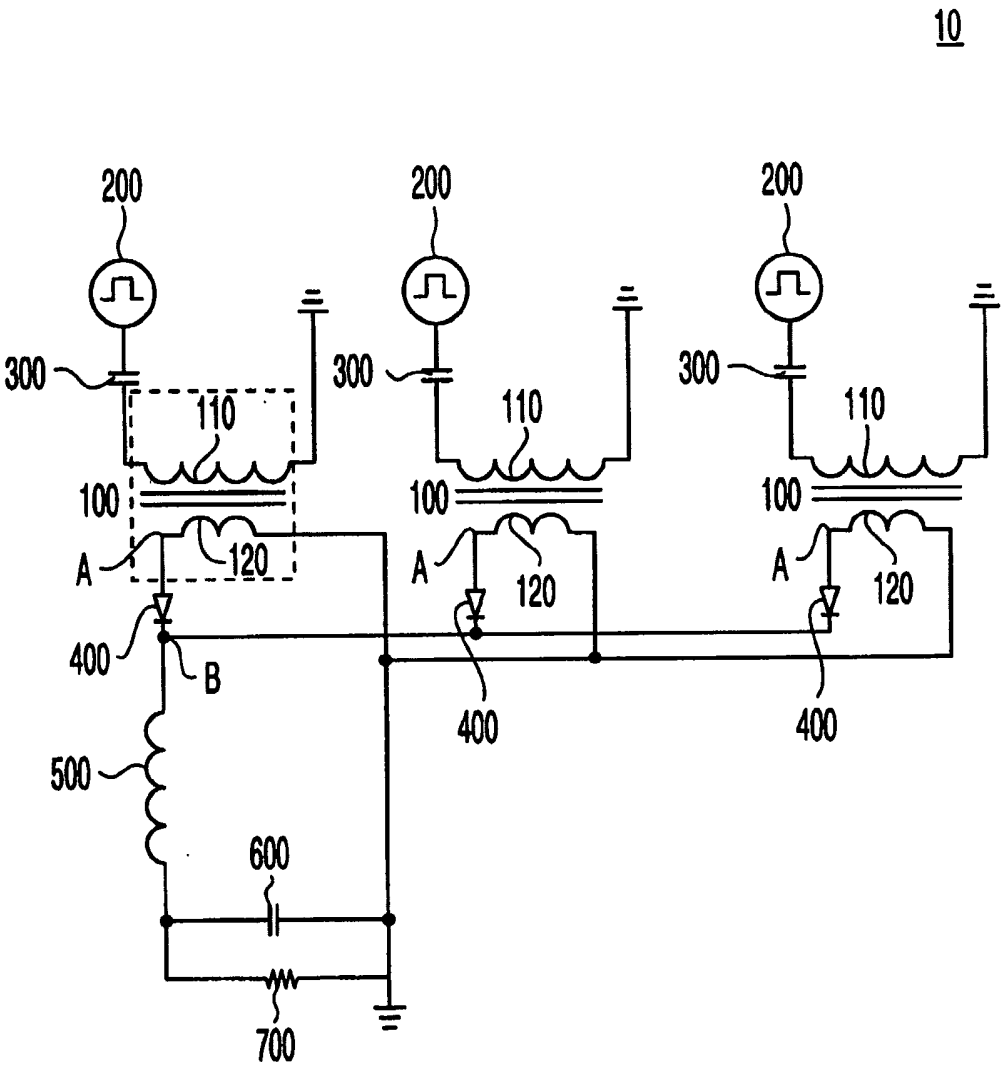

10
200
200
200
300
300
300
110
110
110
100
100
100
A
120
A
120
A
120
400
B
400
400
500
600
700

FIG. 2

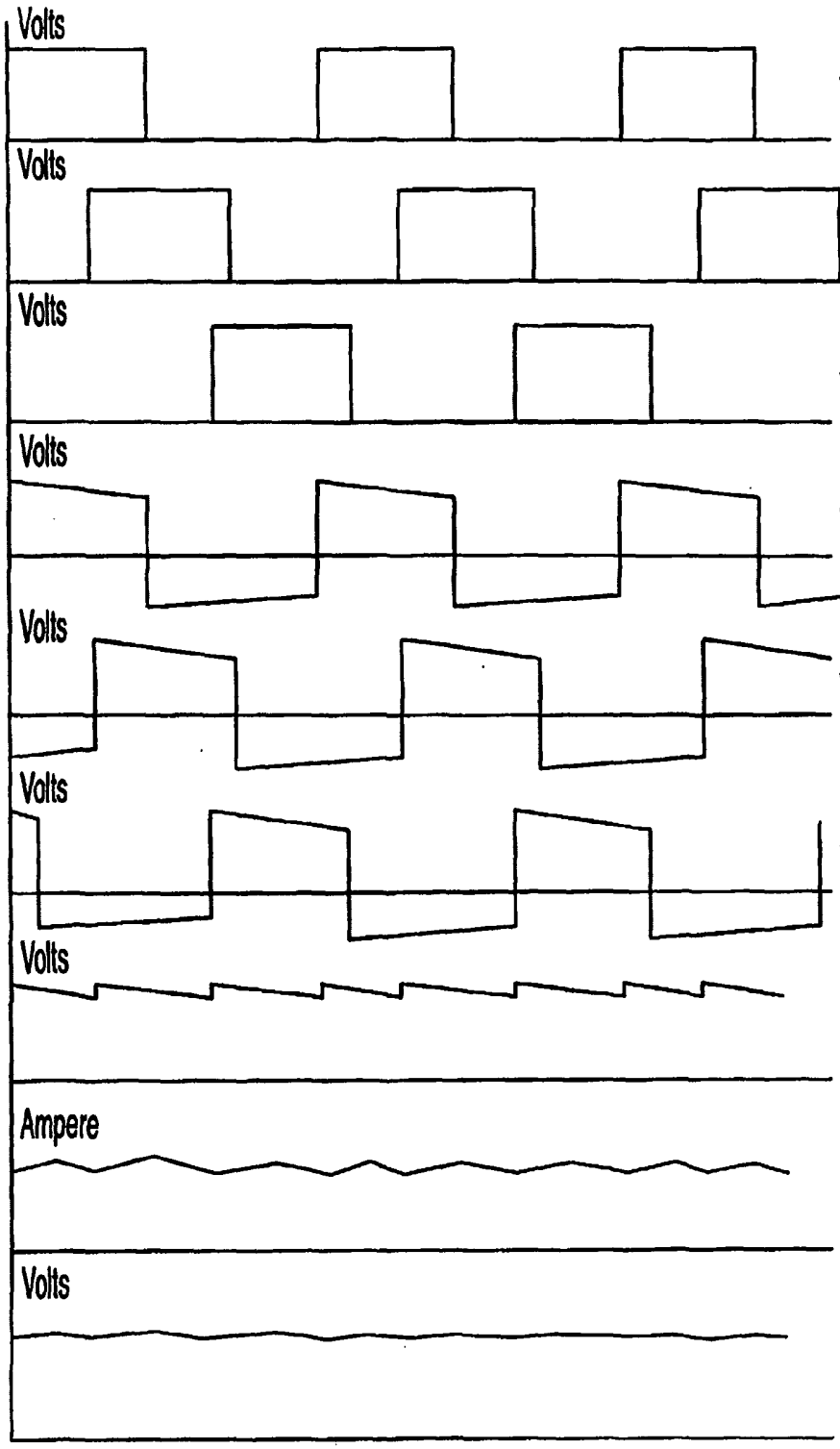


FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 3E

FIG. 3F

FIG. 3G

FIG. 3H

FIG. 3I

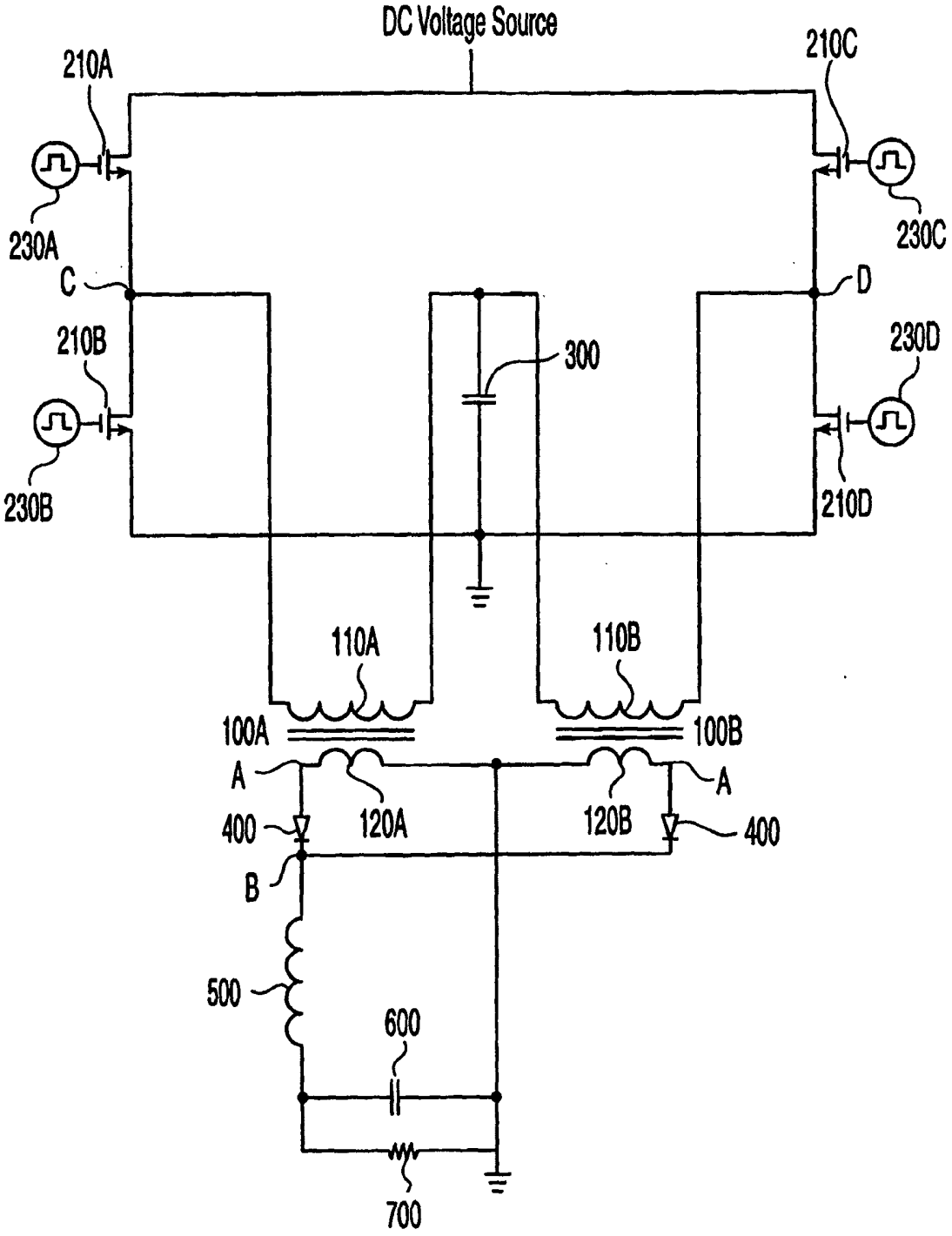

DC Voltage Source
210A
210C
230A
230C
C
D
210B
300
230D
230B
210D
110A
110B
100A
100B
A
A
400
120A
120B
400
B
500
600
700

FIG. 4

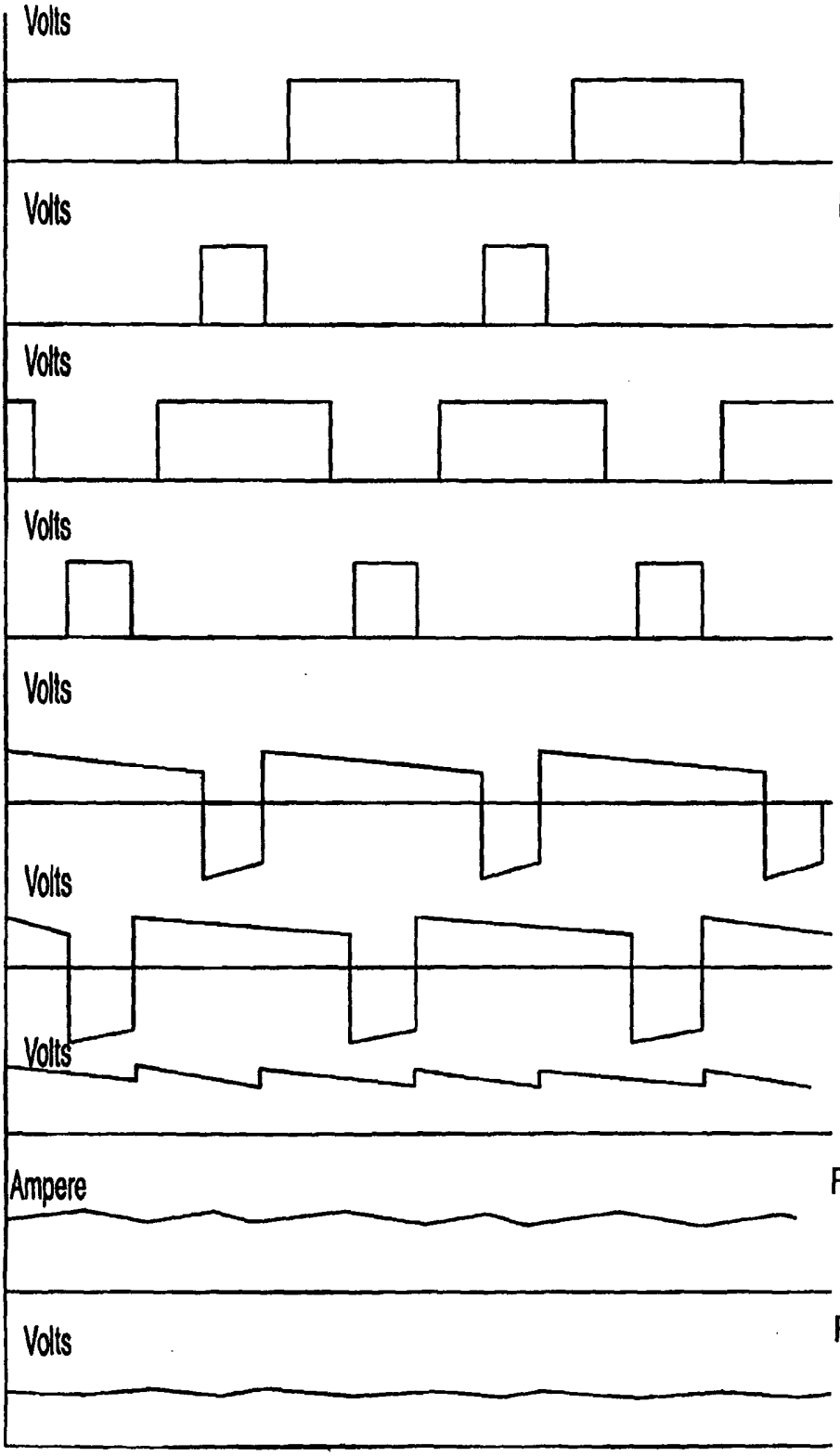


FIG. 5A

FIG. 5B

FIG. 5C

FIG. 5D

FIG. 5E

FIG. 5F

FIG. 5G

FIG. 5H

FIG. 5I

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN02/00920

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H02M7/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7 H02M7/00 H02M3/00 H02J1/00 H02J3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT WPI EPODOC PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN,Y,2453604 (THE UNIVERSITY OF ZHEJIANG) 10. Oct .2001 (10.10. 01) See the whole document	1-28
A	CN,A,1286523 (THE UNIVERSITY OF AVIATION AND SPACEFLIGHT OF NANJING) 7.MAR.2001(07.03.01) See the whole document	1-28
A	US.A.5668646 (THE BOARD OF TRUSTEES OF THE UNIVERTY OF ILLINOIS,URBANA,Ill.) 16.Sep.1997(16.09.97) See the whole document	1-28

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20.Jan.2003(20.01.03)	13 FEB 2003 (13.02.03)
Name and mailing address of the ISA/CN 6 Xitucheng Rd., Jimen Bridge, Haidian District, 100088 Beijing, China Facsimile No. 86-10-62019451	Authorized officer ZHANG , Haichun Telephone No. 86-10-62093820

Form PCT/ISA /210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN02/00920

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5663876 (LUCENT TECHNOLOGIES INC.,MURRAY HILL,N.J.) 2.Sep.1997(02.09.97) See the whole document	1-28
A	US,A,5600546 (COMPUTER PRODUCTS,INC.,BOCARATON,FLA.) 4.Feb.1997(04.02.97) See the whole document	1-28
A	CN,U,86202265 (ENGINERY INDUSTRY DEPARTMENT OF ENGINERY RESEARCH INSTITUTE) 17.Dec.1986(17.12.86) See the whole document	1-28

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN02/00920

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN2453604 Y	10.10.01	NONE	
CN1286523 A	07.03.01	NONE	
US5668464 A	16.09.97	WO9613766 A	09.05.96
		AU4105296 A	23.05.96
US5633876 A	02.09.97	NONE	
US5600546 A	04.02.97	EP0768748 A	16.04.97
		CN1151630 A	11.06.97
		US5652700 A	29.07.97
		JP9266670 A	07.10.97
		US5751561 A	12.05.98
		US5995383 A	30.11.99
CN86202265 U	17.12.86	NONE	