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Power Compensation and Power Quality Improvement Based on Multiple-Channel Current Source Converter Fed HT SMES

Zheng Wang, K. T. Chau, Bo Yuwen, Zhen Zhang, and Fuhua Li

Abstract—The purpose of this paper is to propose the high-performance modulation strategy, power control and current regulation schemes for a multiple-channel current source converter (CSC) fed high temperature (HT) superconducting magnetic energy storage (SMES), which can in turn function as the frequency stabilizer and active power filter for the distributed generation system. The key is to design and implement the interleaved space vector modulation technique to suppress the switching harmonics, the dynamic capacitor voltage control to damp LC resonance as well as regulate grid currents accurately, and the DC current balancing strategy to avoid the circulating currents. The multiple-channel CSC fed HT SMES with the proposed control scheme is verified to provide good performance in power compensation and power quality improvement.

Index Terms—Current balancing, frequency stabilization, HT SMES, multiple-channel CSC, power quality.

I. INTRODUCTION

The applied superconductivity is drawing more and more attention in electric power systems and machines today [1]. Due to the attractive features of high power density, fast charging speed, long life and high efficiency, the high temperature (HT) superconducting magnetic energy storage (SMES) has been used to improve the operating performance of the distributed power generation system. The HT SMES was verified to offer the capability of smoothing the active power [2], enhancing the transient stability [3], and improving the power quality [4]. The HT SMES could be incorporated not only at the AC side but also at the DC side of distributed generation systems [5]. In [6], it indicates the current source converter (CSC) based SMES can provide more reactive power to grid than the voltage source converter (VSC) one under the same active power rating. Besides, the CSC offers the features of simple configuration, low dv/dt, four quadrant operation, and good fault capability for high power applications [7].

Due to the large current in SMES coil and the limited current rating of CSC devices, several CSC channels can be paralleled at the DC side to match the SMES current. At the same time, by connecting CSC channels in parallel at the AC side, the common AC filter can be shared. However, the circulating current will be produced, and unequal DC currents can be resulted in. In [8], the proper operation of carrier signals is designed to balance the DC currents among different channels. But the control schemes of power compensation and current regulation for the system have not been discussed.

The purpose of this paper is to propose and design the high-performance modulation strategy, power control and current regulation schemes for the multiple-channel CSC fed HT SMES. Different from the carrier signal based modulation in [8], the space vector modulation (SVM) is adopted, which offers the advantages of fast dynamics, digital implementation, and high flexibility. In this paper, the interleaved SVM, the dynamic capacitor voltage control, and the dynamic active vector tuning strategy are proposed to improve the operating performance for the multiple-channel CSC fed HT SMES. They are then applied to stabilize the frequency and improve the power quality of power systems.

II. SYSTEM CONFIGURATION & CONTROL SCHEME

A. System Configuration

Fig. 1 shows the configuration of a small power system to study the control schemes for the multiple-channel CSC based HT SMES, where a 15 MVA 4160 V 60 Hz synchronous generator with the governor (GOV) supplies the energy for the load. The 19 MW 35 MJ 5 H HT SMES is connected to the system through the LC filter. A diode fed nonlinear load is incorporated into the system by a circuit breaker (CB). Fig. 2 shows the structure of the multiple-channel CSC HT SMES. The CSC channels
are paralleled at both the AC side and the DC side, and the DC chokes are therefore required to control the DC current for each channel.

B. Power Control and Current Regulation Schemes

Fig. 3 shows the block diagram of the proposed power control and current regulation schemes. The voltage and current are oriented in the direction of the grid voltage with phase lock loop (PLL), resulting the d-axis aligning with the grid voltage and the q-axis orthogonal to it. Thus, the line current reference for the output active and reactive power are $i^*_{ld} = P^*/(1.5v_{id})$ and $i^*_{lq} = Q^*/(1.5v_{iq})$, where $v_{id}$ is the d-axis grid voltage, $P^*$ is the active power reference, and $Q^*$ is the reactive power reference. The current references for the CSC channel are $i^*_{ld} = i^*_{lq} = i^*_{ld} - i^*_{lqd} = i^*_{lq} - i^*_{lq} = i^*_{ld}$, where $i^*_{ld}$ is equal to $i^*_{lq}$ when the diode rectifier fed load is disconnected from the system. The low bandwidth d-axis and q-axis capacitor currents $i^*_{cd}$ and $i^*_{cq}$ are calculated as $i^*_{cd} = -\omega v_{id} C_1$ and $i^*_{cq} = \omega v_{id} C_1$ for the capacitor current compensation, where $\omega$ is the grid frequency, $C_1$ is the filter capacitance, and $v_{id}$ is d-axis grid voltage. In order to suppress the LC resonance, the dynamic capacitor voltage control is used, and thus generates the high bandwidth capacitor references as $i^*_{Dcd} = K_{pvc}(v_{id} - v_{id})$ and $i^*_{Dcq} = K_{pvc}(v_{lq} - v_{lq})$, where $K_{pvc}$ is the control parameter of capacitor voltage controller. The d-axis and q-axis capacitor voltage references $v^*_{id}$ and $v^*_{lq}$ are given by the closed-loop controller of grid currents [7]:

$$v^*_{id} = K_{pvc} (v^*_{id} - i^*_{id}) + K_{i1d} \int (i^*_{id} - i_{ld})$$

$$v^*_{lq} = K_{pvc} (v^*_{lq} - i^*_{lq}) + K_{i1q} \int (i^*_{lq} - i_{lq})$$

where $K_{pvc}$ and $K_{i1}$ are control parameters of grid current controller. Since the total grid current is generated by three CSC channels as shown in Fig. 2, the current references are shared among the three channels.

C. PWM Modulation and DC Current Balance Strategy

The SVM technique is used to modulate the CSC. Fig. 4 shows the vector diagram of SVM for the CSC, where there are six active vectors and three zero vectors. At each instant, the current reference is constructed by two active vectors and one zero vector. For instance, the current reference in sector I can be generated by two active vectors $i^*_{ld}$ and $i^*_{lq}$ and one zero vector $v_{lq}$. To reduce the switching harmonics and improve the total harmonic distortion (THD) performance, the interleaved SVM is proposed by introducing a shifted duration of $T_s/3$ between the sampling instants of every two CSC channels, where $T_s$ is the sampling period. The THD is defined as the ratio of the sum of the power of all harmonic components to the power of the fundamental component.

Since both the DC side and AC side of CSC channels are paralleled, different switching characteristics of devices and electrical parameters of CSC channels may produce unequal DC currents. In [9], the unbalanced DC currents of the two-channel CSC fed motor drive are suppressed effectively by dynamically tuning the dwelling time of active vectors of SVM. In this paper, this current balancing scheme is modified for the CSC fed grid converters, and extended to the multiple-channels. To describe the principle of the proposed current balancing scheme, Table I
TABLE 1
INFLUENCE OF ACTIVE VECTORS ON DC CURRENTS

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<tr>
<td>(v_{A^+V_B})</td>
<td>(-)</td>
<td>(-)</td>
<td>(i_1)</td>
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<tr>
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</tr>
<tr>
<td>(v_{B^+V_C})</td>
<td>(i_2)</td>
<td>(-)</td>
<td>(-)</td>
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<tr>
<td>(v_{B^+V_C})</td>
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</tr>
<tr>
<td>(v_{C^+V_A})</td>
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<td>(v_{C^+V_A})</td>
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lists the influence of active vectors on the positive DC current \(i_1\) and negative DC current \(i_2\) in various sectors. By calculating the error between the DC current of each channel and the average value of the three channels, a simple PI controller is used to tune the dwelling time of the effective active vectors to affect the DC current for each CSC channel.

III. POWER COMPENSATION & POWER QUALITY IMPROVEMENT

With the proposed PWM strategy and control schemes, the HT SMES can regulate the output power accurately. So, the active power in the power system can be compensated well to improve the transient stability. By detecting the grid frequency with PLL and calculating the frequency deviation from the rated value, the required compensating active power \(P^*\) is generated by the frequency stabilizer (FS) through a simple PI controller. As shown in Fig. 3, the sum of \(P^*\) and the original \(P^*\) acts as the total active power reference for the HT SMES.

If the nonlinear load is connected in the power system as shown in Fig. 1, the low order harmonic current is produced and the power quality will be deteriorated. Under this condition, the multiple-channel CSC HT SMES can act as active power filters by purposely injecting the out-phase harmonics into the system. The harmonic calculator (HC) detects the harmonics \(i_{hd}^*\) and \(i_{h0}^*\) by subtracting the fundamental components from the measured system currents. Then, the detected current harmonics \(i_{hd}^*\) and \(i_{h0}^*\) will be subtracted from the original current references for CSCs as shown in Fig. 3, and the out-phase harmonics will be generated by the HT SMES.

IV. SIMULATION VERIFICATION

To verify the performance of the proposed multiple-channel CSC fed HT SMES and control schemes, Matlab/Simulink is used to simulate the power system in Fig. 1. The sampling frequency of each CSC channel is 4.32 kHz, and the corresponding switching frequency is 2.16 kHz. Firstly, the simulated grid current and capacitor voltage waveforms of the SMES are plotted in Fig. 5. As shown in Fig. 5(a), the switching harmonics produces the high frequency ripples in the waveforms when the sampling instants of the three channels are identical. By using the interleaved SVM, Fig. 5(b) indicates the THD performance of the waveforms becomes better.

Secondly, the performance of the power control is verified in Fig. 6 with \(P^*= -5\) MW and \(Q^*= 0\) Mvar. When the high bandwidth current references \(i_{Dc}^*\) and \(i_{Dq}^*\) are not included, the output power deviates from the reference value as shown in Fig. 6(a). On the other hand, the output power can be regulated accurately by including \(i_{Dc}^*\) and \(i_{Dq}^*\) into the current references of CSC as shown in Fig. 6(b) since the closed-loop control of grid current is incorporated.

Thirdly, the performance of the current balancing scheme is given in Fig. 7. By purposely increasing the DC choke inductance in channel 1 and series connecting one additional diode in the DC side of channel 3, the SMES current can not be shared equally among the three channels without any countermeasure before \(t=4\) s. After \(t=4\) s, the DC currents can be balanced effectively due to the proposed current balancing.

Fourthly, the performance of the frequency stabilization with the proposed HT SMES is verified. Fig. 8(a) shows the output power, the speed of synchronous machine, and grid frequency without FS when the 2 MW load is removed from the system by disconnecting the circuit breaker (CB). It can be observed the synchronous generator speed oscillates with the amplitude up to 1.007 pu and the grid frequency goes up beyond 60.4 Hz. By incorporating FS in the control scheme, both the generator speed and the grid frequency are damped well in Fig. 8(b). The speed
Fig. 8. Performance of frequency stabilization: (a) without FS and (b) with FS.

is limited below 1.001 pu while the grid frequency is below 60.1 Hz. It is also observed that the HT SMES reduces its output active power after disconnecting the 2 MW load.

Fifthly, when the diode rectifier fed nonlinear load is connected to the system, the waveform of the total line current of nonlinear load and HT SMES is plotted in Fig. 9. Fig. 9(a) shows the waveform without the load harmonic compensation, and Fig. 9(b) shows that with the load harmonic compensation. The low order harmonics induced by nonlinear load can be well suppressed with the proposed scheme.

V. CONCLUSION

In this paper, the high-performance power control and current regulation schemes have been proposed, designed, and implemented for the multiple-channel CSC fed HT SMES. The interleaved SVM technique with shifted sampling instants is designed for different CSC channels to reduce the switching harmonics. The high bandwidth dynamic capacitor voltage control scheme is given to suppress the LC resonance and implement the closed-loop grid current regulation. The DC current balancing strategy is designed to avoid the circulating current among different channels. Based on simulation, the multiple-CSC fed HT SMES with the proposed control schemes has been verified to offer good operating performance in power compensation and power quality improvement for the distributed generation system.

REFERENCES


