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<td>Xiong, S; Tan, SC; Wong, SC</td>
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Analysis and Design of a High-Voltage-Gain Hybrid Switched-Capacitor Buck Converter

Song Xiong, Siew-Chong Tan, Senior Member, IEEE, and Siu-Chung Wong, Senior Member, IEEE

Abstract—This paper presents an analysis on the effect of having different number of capacitors \( n \) in the first-stage switched-capacitor circuit of an improved hybrid switched-capacitor buck converter for high-voltage-gain conversion. Various aspects of the topology, operation, and efficiency are investigated. It is shown both analytically and experimentally that a higher \( n \) in the step-down capacitor stage does not necessarily lead to an overall improved power efficiency. A design and optimization method is thus proposed for the improved SC-buck converter.

Index Terms—High voltage gain converter, hybrid switch-capacitor buck converter.

I. INTRODUCTION

HIGH-VOLTAGE-GAIN dc-dc converters are commonly used for electronic applications. To save energy, the supply voltage of modern electronics is decreased to an ultra-low voltage level of less than 1 V. Meanwhile, the intermediate dc supply voltage, especially that of renewable power sources [1], is at a relatively high level of above 12 V [2]–[6]. This prompts the power electronics community to investigate high-voltage-gain dc-dc converters which have a low-voltage output and a high bandwidth regulation.

At present, the electronic industry is still using simple and easy-to-control converters based on conventional buck converter topologies, for achieving such kind of voltage step-down conversions [2]–[5]. However, to achieve high-voltage-gain conversions, the buck converter has to be operated with a very small duty ratio \( (D = \frac{V_{out}}{V_{in}} \text{ being very small}) \), which not only complicates its implementation due to the limits of the duty ratio and the switching frequency [6], but also deteriorates its dynamic performance and reduces its efficiency due to the very-short on time and very-long freewheeling time within the switching cycle [7]. For this kind of conversion, converters with transformers would be a better choice. However, this increases size and cost, which makes them less acceptable for applications that do not need isolation [6].

Switched-capacitor (SC) dc-dc converters, which consist exclusively of power switches and capacitors, can efficiently perform high-voltage-gain conversion [6]–[8]. As there is no magnetic component in the topologies, they are suitable for integrated circuit (IC) implementation in microelectronic form. Besides, they also have advantages of small size, light weight, high efficiency and high power density [9]–[17]. These advantages make them useful in modern electronic products such as portable digital assistant, MP3 players, digital cameras, FLASH, and LED lighting applications [18], [19]. However, SC dc-dc converter cannot get a high efficiency if they are used for the purpose of voltage regulation, which limits their applications [9]–[20].

The limitations of the conventional converters have spurred the interests in developing a new kind of high-voltage-gain hybrid SC dc-dc converters [6]–[8], [21]–[25], of which the converter is made up of a first-stage SC converter, followed by a second-stage buck converter. For this two-stage SC-buck converter, the first-stage SC converter steps down the input voltage to a low level while the second-stage buck converter mainly performs the voltage regulation. An overall high efficiency is achievable with such two-stage hybrid SC-buck converter because the first-stage SC converter is used only for voltage transformation and not voltage regulation. As mentioned, for performing only voltage transformation, a very high efficiency SC converter is achievable. Industrial SC converter products of higher than 98% efficiency (e.g., LTC1044, MAX1044, SI7660, GS7660, etc.) is available. Once the input voltage is converted to a low unregulated voltage by the high efficiency SC converter, the second-stage buck converter will perform a small voltage transformation and the voltage regulation operation at a high efficiency. This is also possible because the input voltage to the buck converter is already at a low level making its duty ratio relatively normal. Recall that the reason why a single buck converter when used for high-voltage-gain conversion is lossy is because the buck converter has to do both the voltage conversion and regulation and that its duty ratio being the function of the input voltage and the output voltage, is very small.

Interestingly, while the concept of such converters have been widely reported [6], [7], [21]–[23], the effect of having different number of capacitors \( n \) in the first-stage switched-capacitor circuit has not been studied. In this paper, using an improved hybrid SC-buck converter as an illustrative example, we introduce a systematic way of modifying \( n \) for high-voltage-gain conversion that will result in an optimal way of designing and configuring such a hybrid SC-buck converter. Various aspects of the topology, operation, and efficiency will be discussed.
This paper is organized as follows. Section II shows the modified topology of the SC-buck converter and its working principle. Section III gives an analysis on the efficiency of the converter using an energy-flow approach. Section IV describes the control mechanism of the SC-buck converter. Section V shows the experimental results of the modified circuit. Section VI gives a guideline on the design of the SC-buck converter. Section VII gives the conclusions to this paper.

II. HYBRID SWITCHED-CAPACITOR BUCK CONVERTER

A modified version of the hybrid SC-buck converter that was originally reported in [24] is illustrated in this paper. Using the proposed hybrid SC-buck converter with \( n \) flying capacitors (hereon known only as SC-buck converter), the effect of having a different step-down conversion ratio in the first-stage SC converter on the SC-buck converter is theoretically investigated in this section and experimentally verified in Section V. Some insights to the design of the converter can be obtained from this analysis.

Fig. 1 shows the SC-buck converter and its timing diagram. Fig. 2 shows its three operating states.

In State 1, all \( S \) switches are “ON” and all \( P \) switches are “OFF.” \( V_{in} \) charges the flying capacitors \( C_1, C_2, \ldots, C_n \), which are connected in series as illustrated in Fig. 2(a). Concurrently, the buck stage of the converter is in freewheeling mode, of which the current in \( L \) freewheels through \( S_0 \).

In State 2, all \( S \) switches are “OFF” and all \( P \) switches are “ON.” All the flying capacitors are connected in parallel and discharge to the buck stage of the converter as shown in Fig. 2(b).

In State 3, all switches are “OFF” as indicated in Fig. 2(c). Flying capacitors are neither charging nor discharging. The current in \( I \) freewheels through the body diode of \( S_0 \).

The equivalent circuits of State 1 and State 2 shown in Fig. 3 can be illustrated as given in Fig. 3(a) and (b), respectively, where \( r_{dson} \) is the turn-on resistance of the switch, \( r_{esr} \) is the resistance of each flying capacitor, \( r_{esr-C} \) is the resistance of the output capacitor \( C \), and \( r_{esr-I} \) is the resistance of \( I \).
Fig. 4. Comparison of experimentally measured efficiencies among SC-buck converters with \( n = 2, 3, 4 \) and a buck converter (i.e., \( n = 1 \)).

Table I

<table>
<thead>
<tr>
<th>Parameters of SC-Buck Converter</th>
<th>( V_{in} ) &amp; ( V_{out} )</th>
<th>( f_s )</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 12 , \text{V} ) &amp; ( 1 , \text{V} )</td>
<td>200 kHz</td>
<td>ST7356ADP</td>
<td></td>
</tr>
<tr>
<td>( C_1, C_2, \ldots, C_n )</td>
<td>( L )</td>
<td>( C )</td>
<td></td>
</tr>
<tr>
<td>94 ( \mu \text{F} )</td>
<td>13 ( \mu \text{H} )</td>
<td>410 ( \mu \text{F} )</td>
<td></td>
</tr>
</tbody>
</table>

A prototype based on the SC-buck topology \( \{ n = 2, 3, 4 \} \), given in Fig. 1(a) and parameters given Table I is constructed. The number \( n \) can be modified by connecting or bypassing the single-cell structure depicted in Fig. 1(c). Experiment is performed to compare the performance of this converter against a conventional buck converter. Both the buck converters have the same \( V_{in} \) and \( V_{out} \). Operating at the same 12 V input and 1 V output condition, it can be seen from Fig. 4 that the SC-buck converters give a better efficiency than the conventional buck converter, except when it is at very light-load condition, similar to what has been reported in [7] and [22]. From Fig. 4, it is observed that a higher \( n \) of SC-buck converter always give a better efficiency at heavy load. However, depending on the loading condition, there is an optimal \( n \) that allows the SC-buck converter to achieve the best possible efficiency. In the next section, the efficiency of the SC-buck converter will be studied.

III. EFFICIENCY ANALYSIS

From Fig. 2, the energy-flow mechanism of the SC-buck converter can be seen as having two parts as depicted in Fig. 5. First, in State 1, energy is transferred from the power source \( V_{in} \) to the flying capacitors through the SC-stage with a “charging efficiency” of \( \eta_C \). In this state, energy is temporarily stored in the flying capacitors. Then, in State 2, the energy stored in the capacitors will be transferred to the load through the buck-stage with a “discharging efficiency” of \( \eta_D \). Averaged over a switching period, the energy in the flying capacitors is kept constant during steady state. The overall efficiency of SC-buck converter is the product of the charging efficiency and the discharging efficiency, i.e., \( \eta_{overall} = \eta_C \cdot \eta_D \).

The circuit in Fig. 3(a) can be further simplified into equivalent circuits representing the charging, discharging and free-wheeling operations as given in Fig. 6(a)–(c), respectively. For Fig. 6(a), \( C_{eq,C} = C_1/n = C_{sum}/n^2 \) and \( r_{eq,C} = n \cdot (r_{ds,on} + r_{ext}) \). For Fig. 6(b), \( r_{eq,EF} = r_{ds,on} + r_{ext,i} \). For Fig. 6(c), \( C_{eq,D} = n \cdot C_1 = C_{sum}/n \) and \( r_{eq,D} = (r_{ds,on} + r_{ext})/n \). Here, \( C_{sum} = C_1 + \ldots + C_n \).

A. Charging Efficiency \( \eta_C \)

The charging efficiency \( \eta_C \) given in the energy-flow diagram in Fig. 5 can be obtained by analyzing the \( RC \) circuit given in Fig. 6(a). In this state, the energy stored in the flying capacitors will be transferred to the buck stage in the following state. The energy change would have an influence on the charging efficiency. The key point of calculating charging efficiency is to obtain the initial voltage of the flying capacitors. The method of deriving the charging efficiency of an equivalent \( RC \) circuit of an SC converter is given in [8]. Here, we apply the method to this converter.

First, the voltage across \( C_{eq,C} \) is

\[
V_{eq,C}(t) = V_{in} \left[ 1 - (1 - b) e^{-\frac{t}{\tau}} \right],
\]

where \( b = V_{eq,C}(t)/V_{in} \), \( \tau = r_{eq,C} C_{eq,C} \), and that \( V_{eq,C}(t) \) is the initial voltage of the equivalent flying capacitor. The total energy stored in \( C_{eq,C} \) in each switching period is

\[
\Delta E_C(t) = \frac{1}{2} C_{eq,C} \left( V_{eq,C}^2(t) - V_{eq,C}^2(1) \right).
\]

This stored energy will be discharged into the buck stage. We denote \( \Delta E_T \) as the energy consumed by the buck stage in one period. Therefore, \( \Delta E_C(t_{on}) = \Delta E_T \).

Assume the input power of the buck stage of the SC-buck converter is \( P_{bin} \). In one switching period, the input energy is

\[
\Delta E_T = P_{bin} t = P_{bin}/f_S.
\]
Fig. 7. Properties of SC-stage charging efficiency. (a) Plot of calculated charging efficiency for different $n$. (b) Plot of calculated charging efficiency for different $C_{eq,c}$. (c) Plot of calculated charging efficiency for different $P_{bin}$. (d) Plot of calculated charging efficiency for different switching frequency $f_s$.

At steady state, for each period, the energy stored in $C_{eq,c}$ is equal to this input energy, i.e., $\Delta E_C(T_{on}) = \Delta E_T$, giving

$$V_{eq,c}(T_{on})^2 - V_{eq,c}(t)^2 = \frac{2P_{bin}}{f_s C_{eq,c}}.$$

(4)

By substituting (1) into (4) and solving the equation, the initial voltage can be derived as

$$b = \frac{1}{1 + e^{-\frac{Z_{eq}}{V_o}}} \times \left[ e^{\frac{Z_{eq}}{V_o}} + \sqrt{1 - \frac{2P_{bin} \left( 1 + e^{-\frac{Z_{eq}}{V_o}} \right)}{f_s C_{eq,c} V_o^2 \left( 1 - e^{-\frac{Z_{eq}}{V_o}} \right)}} \right].$$

(5)

By substituting $V_{eq,c}(t) = b \cdot V_{in}$ into the charging efficiency equation in [8] where $\eta_C = (V_{eq,c}(t) + V_{eq,c}(t)) / (2V_{in})$, we get

$$\eta_C = \frac{(1 + b) - (1 - b)e^{-\frac{Z_{eq}}{V_o}}}{2}.$$

(6)

Fig. 7(a) gives the charging efficiency plot obtained from (6) for different $n$ of which the total capacitance is kept constant with $C_{eq,c} = 90 \mu F$ at $P_{bin} = 20 W$ and $f_s = 200 kHz$. Fig. 7(b) illustrates the charging efficiency for different values of $C_{eq,c}$, at $f_s = 200 kHz$, $P_{bin} = 20 W$, $n = 3$, $V_{in} = 12 V$, and $V_o = 1 V$. Fig. 7(c) shows the charging efficiency for different $P_{bin}$ at $f_s = 200 kHz$, $C_{eq,c} = 90 \mu F$, $n = 3$, $V_{in} = 12 V$, and $V_o = 1 V$. Fig. 7(d) shows the charging efficiency for different
switching frequency $f_s$ with $C_{\text{sum}} = 90 \ \mu\text{F}$, $P_{\text{bat}} = 20 \ \text{W}$, $n = 3$, $V_{\text{in}} = 12 \ \text{V}$ and $V_o = 1 \ \text{V}$.

From the calculated results, the following conclusions can be deduced:

1) When the value of capacitor $C_{\text{sum}}$ is fixed, having more flying capacitors gives a lower charging efficiency.

2) With a longer charging time $t_{\text{on}}$ in (6), the charging efficiency $\eta_C$ is higher.

3) A bigger $C_{\text{sum}}$ value leads to a higher charging efficiency. However, the rate of increase in charging efficiency decreases with an increasing $C_{\text{sum}}$.

4) A heavier load gives a lower charging efficiency.

5) A faster switching frequency leads to a higher charging efficiency.

B. Discharging Efficiency $\eta_D$

The discharging efficiency of the SC-buck converter is mainly influenced by the buck stage of the converter, of which it is being used to process and deliver energy from the flying capacitors to the output. Our study shows that the buck-stage efficiency of the SC-buck converter is dominantly the efficiency of a conventional buck converter plus an additional parasitic capacitor charging loss that is not present in the buck converter.

The power loss of buck converter is well documented in many papers. It includes the conduction loss, switching loss, and the ESR loss. In the SC-buck converter, the power loss includes the following losses.

1) Conduction Loss:
   i. Conduction loss on each branch’s switches:

\[
\begin{align*}
P_{c_{\text{sw}_{\text{up}}}} &= R_{\text{dson}}D \left( I_o^2 + \frac{\Delta I_L^2}{12} \right) \quad \text{(upper switch)} \\
P_{c_{\text{sw}_{\text{d}}}} &= R_{\text{dson}}D \left( I_o^2 + \frac{\Delta I_L^2}{12} \right) \quad \text{(lower switch)}
\end{align*}
\]

where $I_o$ is the output current and $\Delta I_L$ is the inductor current ripple.

ii. Conduction loss on the buck-stage switch:

\[
P_{c_{\text{sw}_{\text{sb}}}} = R_{\text{dson}} \left( 1 - D - \frac{2T_{\text{dlt}}}{T_s} \right) \left( I_o^2 + \frac{\Delta I_L^2}{12} \right).
\]

iii. Conduction loss on the body diode of buck-stage switch:

\[
P_{c_{\text{diedr}_{\text{sb}}}} = 2f_S V_{\text{fd}} I_o T_{\text{dlt}},
\]

where $V_{\text{fd}}$ is the forward diode voltage of $S_b$ and $T_{\text{dlt}}$ is the dead time. Thus, the total conduction loss is

\[
P_c = nP_{c_{\text{sw}_{\text{up}}}} + (n - 1)P_{c_{\text{sw}_{\text{d}}}} + P_{c_{\text{sw}_{\text{sb}}}} + P_{c_{\text{diedr}_{\text{sb}}}.
\]

2) Switching Loss:
   i. Switching loss on switches of each branch, which includes the switching loss on the upper switches:

\[
\begin{align*}
P_{c_{\text{sw}_{\text{up}_{\text{on}}}}} &= f_s V_C I_{\text{d}_{\text{on}}} \frac{t_{\text{on}} + t_{\text{off}}}{2} \\
P_{c_{\text{sw}_{\text{up}_{\text{off}}}}} &= f_s V_C I_{\text{d}_{\text{off}}} \frac{t_{\text{on}} + t_{\text{off}}}{2},
\end{align*}
\]

and the switching loss on the lower switches:

\[
\begin{align*}
P_{c_{\text{sw}_{\text{d}_{\text{on}}}}} &= f_s V_C I_{\text{d}_{\text{on}}} \frac{t_{\text{on}} + t_{\text{off}}}{2} \\
P_{c_{\text{sw}_{\text{d}_{\text{off}}}}} &= f_s V_C I_{\text{d}_{\text{off}}} \frac{t_{\text{on}} + t_{\text{off}}}{2},
\end{align*}
\]

where $I_{\text{d}_{\text{on}}}$ and $I_{\text{d}_{\text{off}}}$ are respectively the branch current of the capacitor when $P$ is turned on and off.

ii. Switching loss of the body diode of buck-stage switch:

\[
P_{c_{\text{diedr}_{\text{sb}}}} = f_s C_{\text{os}} V_{\text{f}_{\text{d}}},
\]

where $V_{\text{f}_{\text{d}}}$ is the voltage of flying capacitor when $P$ is turned on. Thus, the total switching loss is

\[
P_{sw} = n(P_{c_{\text{sw}_{\text{up}_{\text{on}}}}} + P_{c_{\text{sw}_{\text{up}_{\text{off}}}}} + (n + 1) \\
\times (P_{c_{\text{sw}_{\text{d}_{\text{on}}}}} + P_{c_{\text{sw}_{\text{d}_{\text{off}}}}}) + P_{c_{\text{diedr}_{\text{sb}}}}.
\]

3) ESR Loss:
   i. Loss on the ESR of inductor:

\[
P_{c_{\text{esr}_{\text{d}}}} = r_{\text{esr}_{\text{d}}} \left( I_o^2 + \frac{\Delta I_L^2}{12} \right).
\]

ii. Loss on the ESR of a flying capacitor:

\[
P_{c_{\text{esr}_{\text{f}}}} = r_{\text{esr}_{\text{f}}} D \left( I_o^2 + \frac{\Delta I_L^2}{12} \right).
\]
Thus, the total ESR loss is

\[ P_{\text{esr}} = P_{\text{esr},U} + nP_{\text{esr},L}. \]  

(17)

4) Parasitic Capacitor Charging Loss: When the SC-buck converter switches from State 3 to State 1, the voltage across all the \( P \) switches will change. This causes the parasitic capacitor of the \( P \) switches to charge up to a certain voltage level, generating an additional charging loss. Fig. 8 shows the simulation voltage and current waveforms of the SC-buck converter during the transition from State 3 to State 1, which introduces the additional power loss.

The equation describing the parasitic capacitor charging loss of each \( P \) switch is given as

\[
\begin{align*}
P_{\text{ad,up}} & = f_v C_{\text{oss}} V_{\text{sw,up}}^2 \quad \text{for upper switches;} \\
P_{\text{ad,dn}} & = f_v C_{\text{oss}} V_{\text{sw,dn}}^2 \quad \text{for lower switches.}
\end{align*}
\]

(18)

where \( V_{\text{sw,up}} \) and \( V_{\text{sw,dn}} \) are respectively the voltages of the upper and lower switches of each branch. For \( n \) number of \( P \) switches, the parasitic capacitor charging loss is

\[ P_{\text{ad}} = P_{\text{ad,up},1} + \ldots + P_{\text{ad,up},n} + P_{\text{ad,dn},1} + \ldots + P_{\text{ad,dn},(n-1)}. \]  

(19)

Finally, the overall power loss of the buck-stage is

\[ P_{\text{dis,loss}} = P_c + P_{\text{sw}} + P_{\text{esr}} + P_{\text{ad}}. \]

(20)

Then, the discharging efficiency of the SC-buck converter is

\[ \eta_D = \frac{P_a}{P_c + P_{\text{dis,loss}}} \times 100\%. \]

(21)

IV. CONTROL MECHANISM OF THE SC-BUCK CONVERTER

As the buck stage of the SC-buck converter is switching between the freewheeling and the discharging operation [see Fig. 6(b) and (c)], it behaves similarly to a simple duty-cycle controlled buck converter. Hence, only an ordinary voltage-mode controller will be needed for the control of the buck stage of the SC-buck converter. With this controller, the compensator can be designed using the pole placement approach. For this work, the adopted controller has a compensation network with the transfer function \( G_c(s) = 5 + (1)/(0.00039s) \). Fig. 9 shows the implementation circuit of the compensation network used in the experimental prototype.

V. EXPERIMENTAL RESULTS

In order to verify the calculation method and the properties of the topology, a prototype has been built. The parameters are shown in Table I. Fig. 10 shows the output voltage waveform of a SC-buck converter with 5 flying capacitors \((n = 5)\) under a constant load of 15 A. In comparison to the flying capacitor voltage of the first-stage SC converter, the final output voltage waveform of the SC-buck converter contains a much smaller voltage ripple.

Fig. 11 depicts the closed-loop output voltage waveforms of the SC-buck converter operating with an active load switching between 0 A and 5 A, showing that ordinary voltage-mode control can be applied to the SC-buck converter with good result.

Fig. 12 gives a comparison of the calculated efficiencies and the experimental efficiencies at various output power levels and value of \( n \). The efficiency curves fit well at higher power levels. The small discrepancy at lower power levels may be due to the relative higher measurement error at the lower power levels.

Fig. 13 gives the experimental efficiency curves at various output power levels using a different \( n \). The results show that
VI. CIRCUIT DESIGN AND OPTIMIZATION

Four parameters are needed to start a design: input voltage ($V_{\text{in}}$), output voltage ($V_o$), maximum output current ($I_{o,\text{Max}}$) and the switching frequency ($f_s$). With these parameters, the component design of the converter circuit can be carried out based on the number of capacitor $n$ chosen, as given in the following subsection.

A. Components Selection

i. Inductor: Assuming that the switch of the buck is ideal, then

$$L = V_o \cdot \left(1 - \frac{V_o}{V_{\text{in}}} \right) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}. \quad (22)$$

where $\Delta I_L = p \cdot I_{o,\text{Max}}$, and $p$ is typically chosen as 0.3.
iii. Output capacitor: The output capacitor dictates the ripple of output voltage. The output voltage ripple is

$$\Delta V_o = \Delta I_L \cdot (ESR + \Delta T/C_o).$$

Rearranging (23), we have

$$C_o = \frac{\Delta T}{\Delta V_o - ESR},$$

where

$$\Delta T = \max\left\{\frac{V_o}{V_m} \cdot \left\{1/(f_s) \cdot (1 - \frac{V_o}{V_m})\right\} \cdot \{1/(f_s)\}\right\},$$

and ESR is the equivalent series resistance of output capacitor. Using (24), the value of the output capacitor is determined. Typically, the output voltage ripple is mainly contributed by the ESR of output capacitor.

iii. Flying capacitor: A proper value of the flying capacitor will improve the charging efficiency. Equation (5) gives the initial voltage $b$, which indicates the minimum voltage of the flying capacitors. Furthermore, it also dictates the charging efficiency. To obtain a high charging efficiency, $b$ should be higher than 0.95. Although (5) can give an exact value of the flying capacitor, it is difficult to solve. A simplified version of this equation is desired. Assume the discharging efficiency is 100%. Then,

$$P_{\text{n,Max}} = \frac{1}{2} \cdot f_s \cdot C_{\text{sum}} \cdot \frac{V_m}{n} - \Delta V_f \cdot \Delta V_f,$$

where $\Delta V_f$ is the voltage drop of flying capacitors. In (25), $\Delta V_f$ is relatively low compared with $(V_m)/(n)$. So, (25) can be simplified as

$$P_{\text{n,Max}} = \frac{1}{2} \cdot f_s \cdot C_{\text{sum}} \cdot \frac{V_m}{n} \cdot \Delta V_f.$$

By rearranging (26) and setting $\Delta V_f = (1 - b) \cdot (V_m)/(n)$, the flying capacitor can be simplified as

$$C_{\text{sum}} = \frac{2 \cdot n^2 \cdot V_o \cdot I_{\text{Max}}}{(1 - b) \cdot f_s \cdot V_{\text{in}}^2}.$$

iv. Switch: Essentially, the maximum voltage and current ratings of the switches can be determined using a scaling function of $n$ multiplied by $V_{\text{in}}$ or $I_{\text{in}}$, as shown in Table IV. Most of the scaling functions are simple factors of $n$. However, the charging currents passing through the switches $(S_1 \ldots S_n)$ are controlled by the circuit. The maximum current passing through these switches is

$$I_{\text{Max}} = \frac{\Delta V_f}{R_{\text{on}}},$$

The parameter $R_{\text{on}}$ not only affects the maximum charging current, but also dictates the time constant $\tau$, which affects the charging time. In order to have a high charging efficiency, the charging time should be at least three times higher than the time constant $\tau$. So,

$$R_{\text{on}} = \frac{n}{3} \cdot C_{\text{sum}} \cdot \left(1 - \frac{n \cdot V_o}{V_{\text{in}}}ight) \cdot \frac{1}{f_s}.$$

Substitute (29) into (28), the maximum current passing through the switches $(S_1 \ldots S_n)$ is given as

$$I_{\text{Max}} = \frac{3 \cdot f_s \cdot C_{\text{sum}} \cdot \Delta V_f}{n \cdot \left(1 - \frac{n \cdot V_o}{V_{\text{in}}}ight)}.$$

B. Design and Optimization of the SC-Buck Converter

In the previous subsection, methods of selecting the components are introduced. Here, the design and optimization procedure will be given as follows.

1) Preset the four design specifications of input voltage $(V_{\text{in}})$, output voltage $(V_o)$, maximum output current $(I_{\text{Max}})$ and the switching frequency $(f_s)$.

2) The maximum number of stages $n_{\text{max}}$ is calculated.

3) For $n = 2$ to $n_{\text{max}}$, components are selected as illustrated in Section VI-A. A best efficiency of this $n$ at a particular loading condition can be found as illustrated in Section III.

4) Based on the results of different $n$’s, an optimal $n$ can be obtained.

VII. CONCLUSION

This paper presents an analysis on the effect of having different number of flying capacitors $n$ in the first-stage SC circuit of an improved SC-buck converter for high-voltage-gain conversion. The analysis shows that a higher $n$ in the SC stage with the same overall capacitance leads to a lower charging efficiency. On the other hand, the buck-stage efficiency is dependent on the operating conditions and design parameters. A higher $n$ leads to a higher discharging efficiency. Since the overall efficiency is the multiplication of the charging efficiency and the discharging efficiency, there will be an optimal $n$ in terms of efficiency for each switched-capacitor buck converter at a particular load. The experimental results confirm the analytical findings. As such, a design and optimization procedure is developed for the hybrid switched-capacitor buck converter for choosing the optimal $n$. It is also shown that the converter can easily be controlled using ordinary voltage-mode control for buck converter.


<table>
<thead>
<tr>
<th>TABLE IV</th>
<th>COMPONENTS’ PARAMETERS</th>
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<tbody>
<tr>
<td><strong>Stages</strong></td>
<td><strong>Inductor</strong></td>
</tr>
<tr>
<td>2-stage</td>
<td>$V_o \cdot \left(1 - \frac{2}{3} \frac{V_{in}}{V_T} \right) \cdot \frac{1}{f_s} \cdot \frac{1}{f_s} \cdot ESR$</td>
</tr>
<tr>
<td>n-stage</td>
<td>$V_o \cdot \left(1 - \frac{2}{3} \frac{V_{in}}{V_T} \right) \cdot \frac{1}{f_s} \cdot \frac{1}{f_s} \cdot ESR$</td>
</tr>
</tbody>
</table>

**Switch $S_1$:**
- $V_{in}$
- $I_{in}$
- $I_o$
- $I_o$

**Switch $S_2$:**
- $V_{in}$
- $I_{in}$
- $I_o$
- $I_o$

**Switch $P_1$:**
- $V_{in}$
- $I_{in}$
- $I_o$
- $I_o$

**Switch $P_{n-1}$:**
- $V_{in}$
- $I_{in}$
- $I_o$
- $I_o$

**Switch $P_n$:**
- $V_{in}$
- $I_{in}$
- $I_o$
- $I_o$

**REFERENCES**


Song Xiong was born in Jiangxi Province, China, in 1985. He received the B.Eng. and M.Eng. degrees in electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2007 and 2009, respectively. He is currently working toward his Ph.D. degree in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong.

From January 2009 to January 2010, he worked as a Research Assistant in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University. His current research interests include high-voltage-gain de-de converters and switched-capacitor converters.
Siew-Chong Tan (S’00–M’06–SM’11) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from the Hong Kong Polytechnic University, Hong Kong, in 2005.

From October 2005 to May 2012, he worked as Research Associate, Postdoctoral Fellow, Lecturer, and Assistant Professor in Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong. From January to October 2011, he was Senior Scientist in Agency for Science, Technology and Research (A*Star), Singapore. He is currently an Associate Professor in Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong. Dr. Tan was a Visiting Scholar at Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, Champaign, from September to October 2009, and an Invited Academic Visitor of Huazhong University of Science and Technology, Wuhan, China, in December 2011. He is the coauthor of the book *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton: CRC, 2011). His research interests are focused in the areas of power electronics, control theories, smart grids, and clean energy technologies.

Dr. Tan serves extensively as a reviewer for various IEEE/IET transactions and journals on power, electronics, circuits, and control engineering.

Siu-Chung Wong (M’01–SM’09) received the B.Sc. degree in physics from the University of Hong Kong, Hong Kong, in 1986, the M.Phil. degree in electronics from the Chinese University of Hong Kong in 1989, and the Ph.D. degree from the University of Southampton, U.K., in 1997.

Dr. Wong joined Hong Kong Polytechnic in 1988 as an Assistant Lecturer. He is currently an Associate Professor in the Department of Electronic and Information Engineering at Hong Kong Polytechnic University, Hong Kong. In 2012, he was appointed as Chutian Scholars Chair Professor at Wuhan University of Science and Technology, Wuhan, by the Hubei Provincial Department of Education, China. He was a visiting scholar at the Center for Power Electronics Systems, Virginia Tech, on November 2008 and Aero-Power Sci-tech Center, Nanjing University of Aeronautics & Astronautics, Nanjing, China on January 2009. His research interests include modeling of power converters, nonlinear analysis of power electronics, LED lighting systems, wind energy systems, and Internet traffic analysis.

Dr. Wong serves actively as a reviewer for several IEEE/IET/International journals on power electronics, circuits and systems, and Internet communications. He is an editor of *Energy and Power Engineering* (EPE) journal since 2010. He is a member of the Electrical College, The Institution of Engineers, Australia.