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Nitrided $SrTiO_3$ as charge-trapping layer for nonvolatile memory applications

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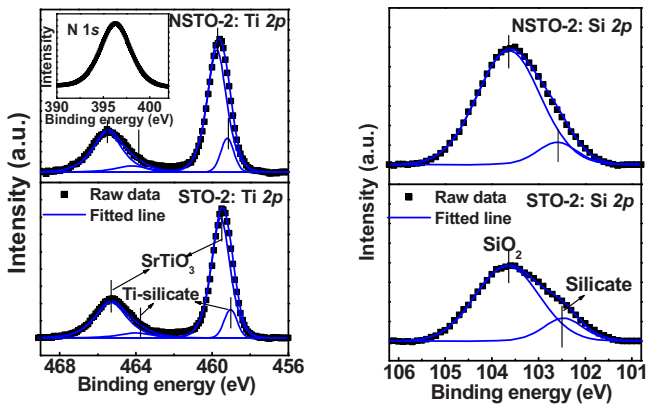
Charge-trapping characteristics of $SrTiO_3$ with and without nitrogen incorporation were investigated based on $Al/Al_2O_3/SrTiO_3/SiO_2/Si$ (MONOS) capacitors. A Ti-silicate interlayer at the $SrTiO_3/SiO_2$ interface was confirmed by x-ray photoelectron spectroscopy and transmission electron microscopy. Compared with the MONOS capacitor with $SrTiO_3$ as charge-trapping layer (CTL), the one with nitrided $SrTiO_3$ showed a larger memory window (8.4 V at ± 10 V sweeping voltage), higher P/E speeds (1.8 V at 1 ms +8 V) and better retention properties (charge loss of 38% after 10^4 s), due to the nitrided $SrTiO_3$ film exhibiting higher dielectric constant, higher deep-level traps induced by nitrogen incorporation, and suppressed formation of Ti silicate between the CTL and SiO_2 by nitrogen passivation. © *2011 American Institute of Physics*. [doi:10.1063/1.3601473]

Charge-trapping nonvolatile (CTN) memories with discrete traps in dielectric for charge storage are regarded as a promising candidate for next-generation nonvolatile memories, due to their lower power consumption, higher reliability, and stronger scaling ability than their floating-gate counterparts. Si_3N_4 is the first dielectric used as the charge-trapping layer (CTL). Recently, extensive researches have been performed to study high-k dielectrics instead of Si_3N_4 as CTL for further scaling down of the memory dimensions and improving its charge-trapping efficiency, e.g., Y_2O_3 ($k \sim 18$),[1] HfON ($k \sim 22$),[2] Pr_2O_3 ($k \sim 15$),[3] Nd_2O_3 ($k \sim 16$),[3] Er_2O_3 ($k \sim 13$),[3] ZrO_2 ($k \sim 37$),[4] and Ta_2O_5 ($k \sim 22$).[5,6] Unfortunately, few dielectrics proposed as CTL show a dielectric constant beyond 30. Moreover, an unavoidable low-k interlayer (e.g., silicate) formed between the high-k dielectric and SiO_2 may further reduce the k value. Among various high-k dielectrics, $SrTiO_3$ is well-known for its high dielectric constant ($k > 140$) and zero band-offset (ΔE_c) with respect to silicon, both of which are desirable as CTL for CTN memories to improve the program/erase (P/E) speeds and retention property.[6–8] However, there have been few reports focusing on $SrTiO_3$ as CTL for nonvolatile memory applications. Furthermore, nitrogen incorporation also plays an important role in the characteristics of $SrTiO_3$ because it may induce more traps in the band gap through substitution of oxygen by nitrogen.[9,10] In addition, the nitrogen incorporation can improve thermal stability and suppress elemental interdiffusion.[6] Therefore, based on MONOS capacitors, this work aims to study the charge-trapping characteristics of nitrided $SrTiO_3$ by comparison with $SrTiO_3$.

MONOS capacitors with $Al/Al_2O_3/SrTiO_3/SiO_2/Si$ were fabricated on p-type silicon substrate. After a standard RCA cleaning, 2 nm SiO_2 was grown on the wafers by thermal dry oxidation. Then, 3 nm $SrTiO_3$ was deposited on the SiO_2 by reactive sputtering using a $SrTiO_3$ target in a mixed Ar/N_2 (4/1) or Ar/O_2 (4/1) ambient, and the corresponding MONOS capacitors were denoted as NSTO-1 and STO-1, respectively. Following that, 10 nm Al_2O_3 was deposited by *in situ* sputtering using an Al_2O_3 target as the blocking layer. Finally, Al was evaporated and patterned as gate electrode, followed by forming-gas annealing at 300 °C for 20 min. $Al/SrTiO_3/SiO_2/Si$ (MNOS) capacitors with and without nitrogen incorporation were also fabricated with the same process, denoted as NSTO-2 and STO-2, respectively. The thickness of the dielectrics was determined by transmission electron microscopy (TEM). The film composition and chemical bonding states were analyzed by x-ray photoelectron spectroscopy (XPS). The electrical characteristics were measured by HP4284A LCR meter and HP4156A semiconductor parameter analyzer.

The atomic content of nitrogen in the NSTO-2 sample is determined to be 8.0% from the XPS analysis shown in the inset of Fig. 1(a). Figure 1(a) shows the Ti $2p$ spectrum and the curve-fitting lines of the NSTO-2 and STO-2 samples. Both of the two samples possess similar spectrum. For the STO-2 sample, The Ti $2p$ spectrum shows two strong peaks located at 465.3 eV (Ti $2p_{1/2}$) and 459.5 eV (Ti $2p_{3/2}$), re-



(a) (b)

FIG. 1. (Color online) XPS spectra of the NSTO-2 and STO-2 samples: (a) Ti $2p$ and (b) Si $2p$. The inset of (a) shows the N $1s$ spectrum of the NSTO-2 sample.

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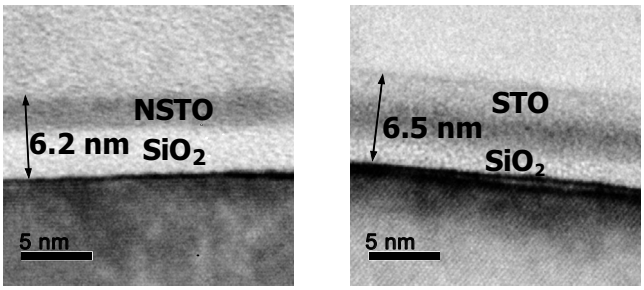


(a) (b)

FIG. 2. TEM cross-sectional image of (a) the NSTO-2 sample and (b) the STO-2 sample.

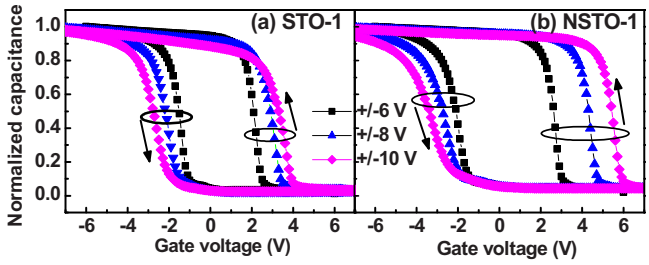


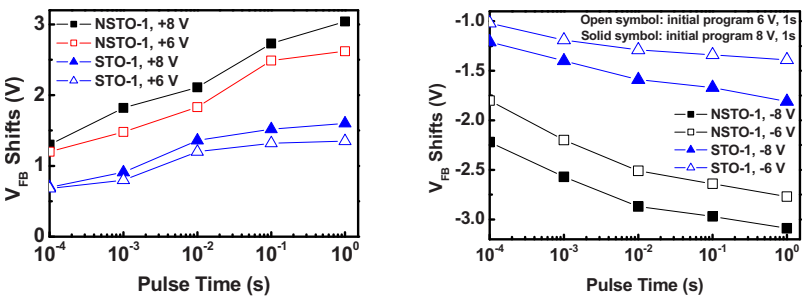
FIG. 3. (Color online) C-V hysteresis curve of the MONOS capacitors under various sweeping voltages: (a) without and (b) with nitrogen incorporation.

spectively. These two peaks are in accordance with the Ti component in $SrTiO_3$ (465.4 eV for Ti $2p_{1/2}$, 459.5 eV for Ti $2p_{3/2}$).[10] Furthermore, two extra peaks are also observed at 464 eV (Ti $2p_{1/2}$) and 459 eV (Ti $2p_{3/2}$), which agree with the values for Ti silicate (464 eV for Ti $2p_{1/2}$, 458.8 eV for Ti $2p_{3/2}$).[11] The presence of Ti silicate can further be confirmed by the Si $2p$ spectrum shown in Fig. 1(b), where the Si $2p$ spectrum in the STO-2 sample exhibits two peaks, corresponding to Ti silicate (102.3 eV) and SiO_2 (103.6 eV), respectively.[11,12] Compared with the STO-2 sample, the Ti spectrum of the NSTO-2 sample displays a chemical shift of 0.2 eV to higher binding energy due to nitrogen incorporation. It is noted that the area ratio of Si component corresponding to SiO_2 and silicate is 8 for the NSTO-2 sample, which is larger than the value ($\sim$5) for the STO-2 one, indicating the formation of thinner Ti silicate in the NSTO-2 sample. Figure 2 shows the cross-sectional TEM image for the NSTO-2 and STO-2 samples. Compared with the NSTO-2 sample, an obvious interlayer is observed in the STO-2 sample. Including the quantum mechanical effect, the equivalent oxide thickness is calculated to be 3.34 and 3.45 nm for the NSTO-2 and STO-2 samples. The dielectric constant of $SrTiO_3$ with and without nitrogen incorporation is evaluated to be 36.7 and 30.3, respectively. Both of the k values are far below the reported value of $SrTiO_3$ ($k>140$), mainly due to the formation of low-k Ti silicate between CTL and SiO_2.[12] The nitrided $SrTiO_3$ film shows higher dielectric constant than the $SrTiO_3$ film due to its thinner interlayer resulting from the nitrogen passivation.

Figure 3 exhibits the 1 MHz C-V hysteresis characteristics of the NSTO-1 and STO-1 samples under various sweeping voltages. As the sweeping voltage increases from $\pm$6 to $\pm$10 V, the memory window increases from 4.6 V/3.6 V to 8.4 V/6.0 V for the NSTO-1 and STO-1 samples, respectively. Compared with the STO-1 sample, the NSTO-1 one shows a larger memory window, which is attributed to its higher dielectric constant and higher trap density resulted from nitrogen incorporation.

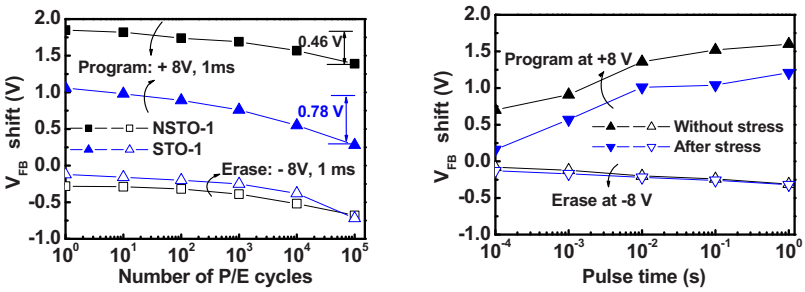
Figure 4 shows the P/E transient characteristics of the NSTO-1 and STO-1 samples at various voltages. For the STO-1 sample, it shows a V_{FB} shift of 0.91 V and 1.60 V at +8 V for 1 ms and 1 s, respectively. For comparison, a larger V_{FB} shift of 1.82 and 3.04 V can be obtained for the NSTO-1 sample under the same operating conditions. Moreover, the NSTO-1 sample still shows a V_{FB} shift of 1.48 V even at a small gate voltage of +6 V for 1 ms, further supporting its higher P/E speeds, due to its high trap density induced by nitrogen incorporation as well as high dielectric constant. The NSTO-1 sample with a thinner interlayer shows higher trap density than the STO-1 one, indicating the traps are mainly distributed in the charge-trapping film rather than the interlayer.

Figure 5(a) shows the endurance characteristics of the MONOS capacitors with $\pm$8 V 1 ms pulse stress. For the NSTO-1 and STO-1 samples, the memory window after 10^5 cycles is 2.13 V and 1.20 V, compared with the initial value of 2.07 V and 1.12 V, respectively, thus only a slight narrowing of memory window after stress for both samples. However, both P/E V_{FB} levels decrease with cycling, which is especially severe for the STO-1 sample. This suggests electron detrapping and/or hole trapping induced by repetitive P/E stress. The P/E transient characteristics of the STO sample before and after 10^4-cycle P/E stress are also shown in Fig. 5(b). The erase characteristics with and without stress coincide well, indicating no extra hole trapping during endurance test. In contrast, the V_{FB} shift after stress is much smaller than that without stress under the program state, demonstrating electron detrapping due to stress-induced defects, which should be responsible for the degradation of the V_{FB} shift shown in Fig. 5(a). Furthermore, the I-V characteristics before and after a 10^5-cycle P/E stress are studied. The STO-1 sample shows larger leakage (6.2 nA/cm^2 and



(a) (b)

FIG. 4. (Color online) (a) Program and (b) erase transient characteristics of the MONOS capacitors. The erase characteristics are measured under an initial program state.



(a) (b)

FIG. 5. (Color online) (a) Endurance characteristics of the MONOS capacitors under ±8 V 1 ms pulse stress. (b) P/E transient characteristics of the STO-1 sample with and without P/E stress.

9.6 nA/cm^2 at V_g=1.5 V before and after stress, respectively) than the NSTO-1 one (6.0 nA/cm^2 and 6.4 nA/cm^2 correspondingly). Larger increase in current for the STO-1 sample indicates more stress-induced defects, which result in more severe degradation of the V_{FB} shift in Fig. 5(a). In addition, a slight over-erase phenomenon can also be observed in Fig. 5(b), which can be explained by some holelike traps existing in the CTL.

Figure 6(a) shows the retention characteristics tested at room temperature with an initial 1 s +8 V program state. The memory window after 10^4 s remains 62% and 49% for the NSTO-1 and STO-1 samples, respectively. The retained charge after 10 years is evaluated to be 27% for the NSTO-1 sample while that of the STO-1 sample is fully closed after 2×10^7 s (0.6 year). The charge loss through the tunneling layer and blocking layer is responsible for the degradation of the memory window during retention period. The formation of the interlayer consumes SiO_2. Furthermore, the Ti-rich silicate shows much smaller barrier height ($E_g\sim3.5$ eV) than SiO_2 ($E_g\sim9.0$ eV), which can enhance charge loss during the retention period.[6,13] The charge-loss mechanism due to the interlayer can further be illustrated by the band diagram shown in Fig. 6(b). The electron-tunneling path from

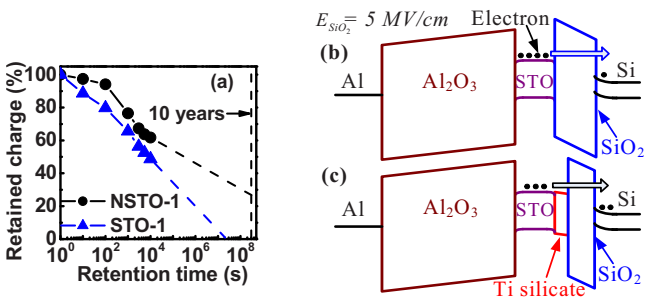


FIG. 6. (Color online) (a) Retention characteristics of the MONOS capacitors measured at room temperature. (b) Band diagram of the MONOS capacitor with no interlayer between $SrTiO_3$ and SiO_2 (Al_2O_3/$SrTiO_3$/SiO_2 =10 nm/3 nm/3 nm). (c) Band diagram with an interlayer between $SrTiO_3$ and SiO_2 (Al_2O_3/$SrTiO_3$/Ti silicate/SiO_2=10 nm/3 nm/1 nm/2 nm).

$SrTiO_3$ to Si is reduced due to the Ti silicate, thus leading to severer charge loss. Consequently, a thinner Ti silicate between the CTL and SiO_2 in the NSTO-1 sample contributes to the better retention property as mentioned above. Moreover, the deep traps induced by nitrogen incorporation should be also desirable for the better retention property.[2]

In summary, the charge-trapping characteristics of $SrTiO_3$ with and without nitrogen incorporation are investigated based on MONOS capacitors. The MONOS capacitor with nitrided $SrTiO_3$ as CTL shows larger memory window, higher P/E speeds and better retention properties than the sample with $SrTiO_3$ as CTL because the nitrided $SrTiO_3$ film exhibits high dielectric constant, large quantity of traps induced by nitrogen incorporation, and suppressed interlayer by nitrogen passivation. Therefore, the nitrided $SrTiO_3$ film is demonstrated to be a promising CTL for high-density nonvolatile memory applications.

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