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Magnetic Instruments

Novel Silicon-Embedded Coreless Transformer for On-Chip Isolated Signal Transfer

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Abstract—In this letter, a novel silicon-embedded coreless transformer is proposed and demonstrated. The transformer is fabricated in the thick bottom layer of a silicon substrate and connected to the frontside through vias opened in the thin top layer where all other components of the system can be fabricated. A 5-turn coreless transformer fabricated using this monolithic transformer technology achieves a small area of 2 mm² and a good voltage gain of larger than –0.8 dB (load = 50 Ω, best reported so far) from 12 to 100 MHz. This technology shows great potential for on-chip isolated signal transfer.

Index Terms—Magnetic instruments, integrated circuits, isolation technology, transformers.

I. INTRODUCTION

Recently, there has been an increasing interest in developing monolithic magnetic components for achieving higher level system integration and miniaturization. In the case of inductor, quite a few monolithic inductors have been reported for RFIC, microelectromechanical systems, and power electronic applications [Ahn 1998, Lin 2005, Wu 2011]. In the case of transformer, a lot of monolithic transformers have been reported for RFIC applications [Long 2000]; however, efforts are still needed to develop good monolithic transformers for isolated signal and power transfer. Isolated signal transfer is needed in many applications, in which the environment is rather noisy. For on-chip isolated signal transfer, monolithic transformers are required to have small size, good voltage gain, and proper operating frequency range. Small size is needed for miniaturization and cost reduction; it also helps to reduce the impact of external noise on the transformer. Good voltage gain is needed to ensure that the output signal is indeed generated from the input signal and not from the noisy environment. Proper operating frequency range is needed in order to correctly transfer a signal, resulting in a proper pulse width and a shape of the original waveform. However, most of the currently reported microtransformers are still too large (>10 mm²) to be monolithically integrated and have low voltage gains (<−3 dB) [Mino 1996, Xu 1998, Park 2003]. The best voltage gain reported previously is −1 dB; however, it is achieved by a 24 mm² microtransformer [Wang 2007]. On the other hand, small-size integrated transformers (<2 mm²) have been reported; however, they need to be operated at hundreds of megahertz due to the small inductance and large resistance [Kurata 1993, Chen 2008]. This high operating frequency makes the pulse width of the transferred signal to be less than 10 ns, which is not long enough to ensure the proper function of the secondary circuitry in many applications. Moreover, the reported small-size integrated transformer has a voltage gain of only −2.7 dB.

In this letter, a novel silicon-embedded coreless transformer (SECT) is demonstrated for on-chip isolated signal transfer. With the novel silicon-embedded design, high level of integration, small footprint, and good voltage gain over a reasonable frequency range are achieved.

II. TRANSFORMER DESIGN AND FABRICATION

A. Transformer Design

For on-chip isolated signal transfer, monolithic transformers are required to have small size, good voltage gain, and proper operating frequency range. In general, in order to achieve a good voltage gain, transformers are required to have small coil ac resistance and good coupling factor. The detailed analysis of the voltage gain dependence on coil resistance and coupling factor has been reported [Mino 1996]. Transformers are also required to have large coil inductances for low-frequency operation. Therefore, a good monolithic transformer for on-chip isolated signal transfer should have small footprint, small coil ac resistance, good coupling factor, and large coil inductance.

Fig. 1 shows the schematic 3-D view of the SECT. Two symmetric interleaved spiral metal coils are placed in the thick bottom layer of a silicon substrate, while the top layer is left for putting all other components of the system as well as to provide sufficient mechanical support. Good coupling factor can be achieved with the interleaved design. Small coil ac resistance can be achieved with thick metal coils, which lead to small dc resistance, and with narrow metal tracks and proper operating frequency, which ensures that the skin effect and the proximity effect are not too significant. Large coil inductance and small footprint are achieved by using small coil track width and spacing. A 2 mm² SECT was designed with two 5-turn interleaved...
circular spiral Cu coils. The other design parameters of the SECT are: outer radius $= 700 \, \mu\text{m}$, Cu track thickness $= 100 \, \mu\text{m}$, Cu track width $= 15 \, \mu\text{m}$, and Cu track spacing $= 10 \, \mu\text{m}$.

B. Transformer Fabrication

The fabrication of the SECT is based on the silicon-embedded coreless power inductor technology previously reported by the authors [Wu 2011]. The fabrication started with a 315 $\mu\text{m}$-thick, 17 $\Omega \cdot \text{cm}$, double-side-polished silicon wafer. After deposition of 3 $\mu\text{m}$ low-temperature oxide (LTO) from both sides of the wafer as the masking material, trenches were etched in the silicon substrate by deep-silicon reactive-ion etching. Trenches, which are 15 $\mu\text{m}$ wide and 100 $\mu\text{m}$ deep were formed from the backside of the wafer for the coils, and 30 $\mu\text{m}$-wide, 215 $\mu\text{m}$-deep silicon trenches were formed from the frontside for the vias. The alignment of the front and back trenches were achieved with a double-sided contact aligner. Three micrometer of LTO was then deposited from both sides of the wafer to cover the exposed silicon surface for isolation. After sputtering of 100 nm TiW and 2 $\mu\text{m}$ Cu from both sides of the wafer as seed layer, Cu electroplating was then performed from both sides of the wafer to fill up the trenches. After that, the overplated Cu at the backside of the wafer was removed by polishing. The overplated Cu at the frontside was also polished to form a flat surface. Finally, pads were formed at the frontside by masked wet etching of the remaining flattened, overplated Cu layer. Fig. 2 shows the SEM images of the cross-sectional view of the Cu filled trenches and the bottom view of the fabricated SECT. Fig. 2(a) was obtained from a test structure for easy cross sectioning of vias. The four miniature spirals at the terminals of the coils are used to increase the cross sectional area of the vias for small via resistance.

III. EXPERIMENTAL RESULTS

The dc resistances of the SECT coils were found to be 0.44 $\Omega$ and 0.45 $\Omega$ by on-wafer four-point probe measurements, with a measured electroplated Cu resistivity of 3.9 $\mu\Omega \cdot \text{cm}$. This resistivity is higher than the typical value of 1.7 $\mu\Omega \cdot \text{cm}$, which is due to the nonoptimized copper electroplating process used. The dc breakdown voltage of the SECT was found to be 20 V, although breakdown strength of 600 V/$\mu\text{m}$ has been reported for LTO [Nam 2007]. This low dc breakdown voltage is due to the nonoptimized oxide deposition process used (poor conformity and low oxide quality). Fig. 3 shows the open-circuit performance of the SECT obtained by one-port on-wafer measurement using R&S ZVB8 vector network analyzer. The open-circuit coil inductance is 35 nH at low frequency, and is larger
than 30 nH up to 100 MHz. A resonant peak is observed at 70 MHz, and the self-resonant frequency is around 280 MHz. This resonance is due to the parasitic capacitance between the Cu coil and the silicon substrate. Fig. 4 shows the voltage gain of the SECT obtained by performing two-port on-wafer measurement. The voltage gains with a load of 50 Ω and with the secondary open (load impedance infinite) are calculated using the following equation, where $Z_L$ is the load impedance and $Z_{11}$, $Z_{12}$, $Z_{21}$, and $Z_{22}$ are the measured two-port Z parameters [Wang 2007]:

$$V_G = \frac{V_{OUT}}{V_{IN}} = \left| \frac{1}{(Z_{11}/Z_{22}) + (Z_{22}Z_{11})/(Z_{21}Z_{L}) - (Z_{12}/Z_{L})} \right|.$$

(1)

It can be seen that with a load of 50 Ω, the voltage gain of the SECT is larger than -0.8 dB over a wide frequency range of 12 to 350 MHz. This is the best voltage gain reported so far. Considering the decrease of the coil inductance beyond 100 MHz, the SECT can be operated from 12 to 100 MHz, with a coil inductance larger than 30 nH and a voltage gain larger than -0.8 dB. This operating frequency range allows signals with pulse width, of tens of nanoseconds to be properly transferred, and therefore, is more reasonable than the hundreds of megahertz operating frequency range of the previously reported small-size transformers [Kurata 1993, Chen 2008]. Over 100 MHz, fluctuations can be observed in the voltage gain of the SECT. This can be explained by the fact that over 100 MHz, the coil inductance of the SECT decreases rapidly and self-resonance is reached, making the transformer voltage gain not meaningful. The low-frequency coupling factor $k$ of the SECT is estimated to be 0.96. Table 1 compares the performance of the SECT with the prior art for on-chip isolated signal transfer. It can be seen that the SECT achieves the best voltage gain reported so far within a small footprint of 2 mm² and with a reasonable operating frequency range of 12 to 100 MHz.

### IV. CONCLUSION

A novel SECT was proposed and experimentally demonstrated. This transformer can be effectively integrated with the entire IC for significant chip area saving. The SECT shows a voltage gain of -0.8 dB, which is the best reported so far, over a reasonable frequency range of 12 to 100 MHz; while only a small area of 2 mm² is needed. This novel transformer shows great potential for efficient on-chip isolated signal transfer applications.

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