Fabrication and Electrical Characterization of MONOS Memory with Novel High-κ Gate Stack

L. Liu, J. P. Xu*, C. L. Chan, P. T. Lai*

Abstract – **A novel high-κ gate stack structure with $HfON/SiO_2$ as dual tunneling layer (DTL), AlN as charge storage layer (CSL) and HfAlO as blocking layer (BL) is proposed to prepare the charge-trapping type of MONOS non-volatile memory device by employing in-situ sputtering method. The memory window, program/erase and retention properties are investigated and compared with similar gate stack structure with Si_3N_4/SiO_2 as DTL, HfO_2 as CSL and Al_2O_3 as BL. Results show a large memory window of 3.55 V at P/E voltage of +8 V/-15 V, high program/erase speed and good retention characteristic can be achieved using the novel Au/HfAlO/AlN/$(HfON/SiO_2)$/Si gate stack structure. The main mechanisms lie in the enhanced electron injection through the high-κ $HfON/SiO_2$ DTL, high trapping efficiency of the high-κ AlN material and effective blocking role of the high-κ HfAlO BL.**

Keywords: MONOS memory, high-κ gate stack, charge storage layer, tunneling layer, blocking layer

I. INTRODUCTION

The challenges for non-volatile memory devices are to achieve fast program/erase (P/E) speed at low operating voltage, large memory window and good 10-year data retention simultaneously [1]. Because of the advantages in scaling, simple fabrication process and robustness against defect-related leakage, metal–oxide -nitride-oxide-silicon (MONOS) memory devices become attractive candidates [2]. Extensive researches have been performed in recent years, involving the use of high-κ HfO_2 [2-3] or AlN [1], [4-5] as charge storage layer (CSL), the use of Si_3N_4/SiO_2 [2] or ZrO_2/SiO_2 [6] as dual tunneling layer (DTL) to enhance the tunneling current, the use of Al_2O_3 as the blocking layer (BL) instead of SiO_2 [7-8] and the use of high-work-function metal gate [9-10] for suppressing electron injection from gate electrode. However, less work concentrated on combining the advantages of high-κ BL and CSL with the dual high-κ/SiO_2 band-engineered tunneling layer. In this paper, we report a novel high-κ gate stack structure --- Au/HfAlO/AlN/$(HfON/SiO_2)$/Si for MONOS memory application which combines a new DTL of $HfON/SiO_2$ with the high-κ HfAlO BL and AlN CSL to comprehensively improve the performances of the devices. The electrical characteristics of this novel device are evaluated through comparison with the similar high-κ gate stack structure of Au/Al_2O_3/HfO_2/(Si_3N_4/SiO_2)/Si. Experimental results indicate that large memory window, fast program/erase speed at low operation voltage and good retention property can be obtained using this novel high-κ gate stack structure.

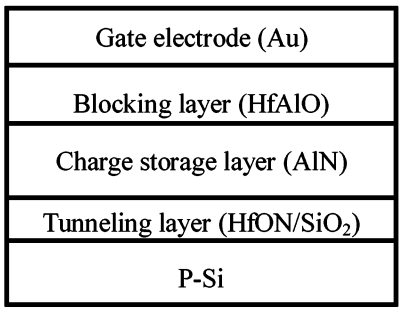

Fig. 1 Schematic cross-section of proposed gate stack.

II. DEVICE FABRICATION

Fig. 1 is the schematic cross-section of gate stack of MONOS memory device. To improve the P/E characteristics of MONOS flash memory device, a new high-κ stack gate dielectric structure of Au/HfAlO/AlN/$(HfON/SiO_2)$/Si is proposed, with $HfON/SiO_2$ as double tunneling layer, AlN as charge-storage layer and HfAlO

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as block layer, as shown in Table I. These high-κ dielectrics were consecutively deposited in-situ by reactive sputtering (or co-sputtering) method using Denton Vacuum Discovery Deposition System at room temperature. First, a 3-nm thick SiO_2 was thermally grown in dry O_2 at 900 ^{0}C on p-type Si substrate with a resistivity of 5-10 Ωcm. Then, a nominal 6-nm HfON was deposited by reactive sputtering of Hf in an Ar/N_2 (24:6) ambient, followed by the deposition of a nominal 12-nm AlN by reactive sputtering of Al in an Ar/N_2 (24:6) ambient, followed by the deposition of a nominal 10-nm HfAlO by reactive co-sputtering of HfO_2 and Al in Ar ambient (24 sccm). A post-deposition annealing (PDA) was carried out in N_2 at 700 °C for 60 s to improve the dielectric quality. For obtaining densification and high-quality tunneling layer and especially blocking layer, their deposition rates were set at low values of 0.125 nm/min and 0.1 nm/min respectively. On the contrary, the charge-storage layer was deposited at a higher rate of 2 nm/min so that more deep-level traps can be formed during deposition. For comparison, a normal high-κ gate dielectric stack of $Au/Al_2O_3/HfO_2/(Si_3N_4/SiO_2)/Si$ (as control sample) was prepared using the same deposition procedure, with a nominal 6-nm Si_3N_4 RF-deposited using Si_3N_4 target at a rate of 0.1 nm/min in Ar (24 sccm), a nominal 12-nm HfO_2 RF-deposited using HfO_2 target at a rate of 0.17 nm/min in Ar (24 sccm) and a nominal 10-nm Al_2O_3 RF-sputtered using Al target at a rate of 0.084 nm/min in Ar/O_2 (24/6) ambient. For avoiding the crystallization of HfO_2, the PDA was performed at 500 ^{0}C for 120 s in N_2. Finally, the high-work-function Au was evaporated and patterned as gate electrode and then Al was evaporated as back electrode, followed by forming-gas annealing which was completed in H_2/N_2 (5% H_2) for 20 min at 400 °C.

For evaluating the memory window and programming/erasing characteristics, high-frequency (1-MHz) C-V curves were measured using HP4284A precision LCR meter, and the programming/erasing voltages were applied by HP4156A precision semiconductor parameter analyzer. The flat-band voltage was extracted from the measured C-V curves by assuming C_{fb}/C_{ox} = 0.5 (C_{fb} and C_{ox} are the flat-band and oxide (or accumulation) capacitances respectively).

Table I

HIGH-κ GATE DIELECTRIC STACK STRUCTURE

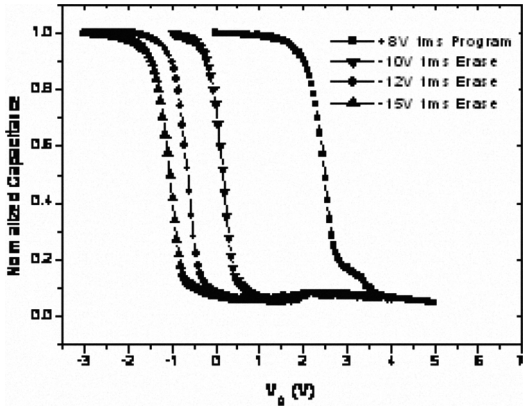
	New device	Control device
Gate	Au	
Blocking layer	HfAlO(10 nm)	Al_2O_3 (10 nm)
Charge-storage layer	AlN (12 nm)	HfO_2 (12 nm)
Dual tunneling layer	HfON (6 nm)	Si_3N_4 (6 nm)
	SiO_2 (3 nm)	SiO_2 (3 nm)

III. RESULTS AND DISCUSSION

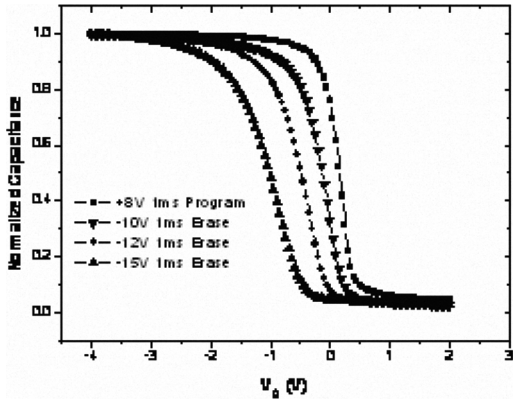
A. Memory window and program-erase performance

The memory window is determined from shift of the flat-band voltage which is extracted from the measured C-V curves under different P/E voltages. As can be seen from Fig. 2, the memory window of the novel device at P/E voltages of + 8 V/- 10 V, + 8 V/- 12 V, + 8 V/- 15 V is 2.35 V, 3.15 V and 3.55 V, respectively, and it becomes 0.35 V, 0.75 V and 1.35 V under the same P/E voltages for the control device. The larger memory window even at low program voltage for the novel device than the control device should be ascribed to the high trapping capability of high-κ AlN charge-storage layer [4] and suitable double tunneling layer structure.

The program/erase performances are evaluated in terms of the flatband-voltage change (ΔV_{fb}) by applying a P/E voltage of +/- 10 V or 15 V for 100 μs. As shown in Table II, larger ΔV_{fb} is obtained for the novel device than the control device under both the same program voltage and the same erase voltage, indicating higher program and erase speeds for the former than the latter. Since the P/E mechanisms are controlled by FN tunneling, the faster programming is due to the higher κ value of HfON than Si_3N_4, which results in higher electric field in SiO_2 and thus enhanced carrier injection from the substrate to the charge-storage layer, and on the other hand, it probably means a smaller ΔE_C of HfON-Si than Si_3N_4-Si. The high erase speed is attributed to the effective blocking role of the high-κ HfAlO blocking layer, which reduces the electron injection from the gate into the AlN charge storage layer during erasing, and small equivalent oxide thickness of the $HfON/SiO_2$ double tunneling layer, which enhances the hole injection from the substrate.



(a)



(b)

Fig. 2 C-V curve of the novel device (a) and control device (b) at different P/E voltages for 1 ms.

TABLE II
CHANGE OF V_{fb} AFTER P/E OPERATION FOR 100 μs

	Program		Erase	
	+ 10 V	+ 15 V	- 10 V	- 15 V
Novel device ΔV_{fb}/ V	+ 0.9	+ 1.35	- 1.05	- 1.4
Control device ΔV_{fb}/ V	+ 0.4	+ 0.7	- 0.5	- 1.05

B. Program-erase retention characteristics

Long retention after programming or erasing is important for non-volatile memory devices. Presented in Fig. 3 is the retention characteristic of $+V_{fb}$ and $-V_{fb}$ extracted from the C-V curves of the two devices measured after programming or erasing at +15 V or -15 V for 1 ms. The retention characteristic is evaluated by measuring the C-V curves after removing the program or erase voltage for 1 - 10000 s. Obviously, a small V_{fb} variation is observed for the novel device with an initial memory window of 3.35 V, which gives an extrapolated 10-year memory window of 2.1 V. The good retention characteristics are due to the strong Al-N bonds related to better trapping capability [5] and deeper trap levels. Also, the suitable high-κ HfAlO blocking layer and HfON tunneling layer, which have reasonable barrier height when contacting with AlN respectively, are responsible for the good retention.

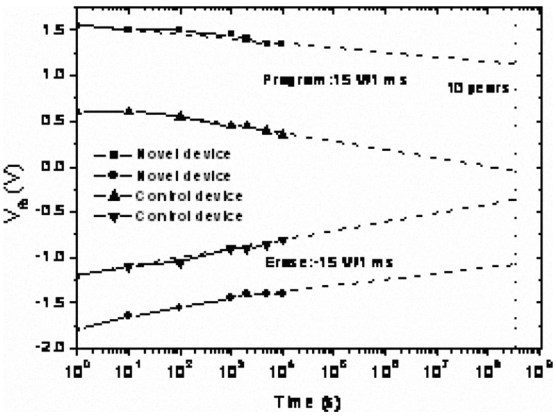


Fig. 3 Comparison of retention property for the two devices after programming or erasing at +15 V or -15 V for 1 ms.

IV. Conclusion

A novel high-κ gate stack structure of Au/HfAlO/AlN/(HfON/SiO_2)/Si for non-volatile MONOS memory device application is fabricated by in-situ sputtering. Comparing with the Au/Al_2O_3/HfO_2/(Si_3N_4/SiO_2)/Si gate stack structure, the novel device exhibits a large memory window of 3.55 V at a P/E voltage of +8 V/-15 V, high program/erase speed and good retention characteristic with an extrapolated 10-year memory window of 2.1 V. The large memory window is related to the effective AlN charge storage layer with more deep-level traps. High P/E speed is attributed to the suitable HfON tunneling layer with higher k value and small conduction-band offset, and effective blocking role of the HfAlO blocking layer. Good retention property lies in the reasonable barrier-height match between the AlN charge-storage layer, HfAlO blocking layer and HfON tunneling layer.

Therefore, the Au/HfAlO/AlN/(HfON/SiO_2)/Si gate stack structure is a promising candidate for making high-performance non- volatile MONOS flash memory devices.

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